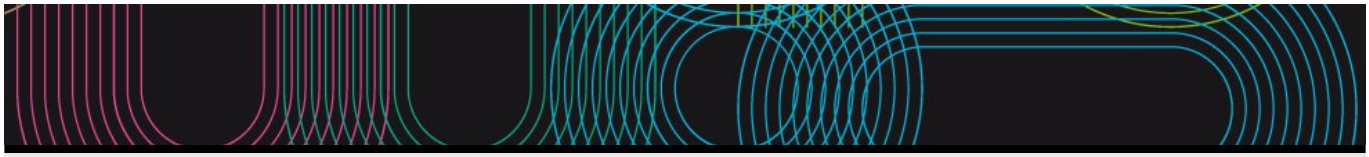

IDENTIFYING DATA				
(*)Codeseño Hardware/Software de Sistemas Empotrados				
Subject	(*)Codeseño Hardware/Software de Sistemas Empotrados			
Code	V05M145V01242			
Study programme	(*)Máster Universitario en Enxeñaría de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	5	Mandatory	1st	2nd
Teaching language	Spanish Galician English			
Department				
Coordinator	Álvarez Ruíz de Ojeda, Luís Jacobo			
Lecturers	Álvarez Ruíz de Ojeda, Luís Jacobo Poza González, Francisco			
E-mail	jalvarez@uvigo.es			
Web	http://www.faitic.uvigo.es			
General description	The documentation of the subject will be in English. Some lectures could be given in English. The main learning goals of this course are: □ To learn the codesign methods to design applications based on embedded microprocessors in FPGAs. □ To get to know the microprocessors that can be implemented in commercial FPGAs. □ To handle the necessary software tools for the development of embedded applications by means of FPGAs. □ To design application specific peripherals and their connection to the buses of the embedded microprocessors. □ To design real applications with embedded microprocessors in FPGAs.			

Competencies	
Code	
A5	CB5 Students must have learning skills to allow themselves to continue studying in largely self-directed or autonomous way
A6	CG1 The ability to project, calculate and design products, processes and facilities in telecommunication engineering areas.
A13	CG8 The ability to apply acquired knowledge and to solve problems in new or unfamiliar environments within broader and multidiscipline contexts, being able to integrate knowledge.
A29	CE11 The knowledge of hardware description languages for high complexity circuits.
A30	CE12 The ability to use programmable logic devices, as well as to design advanced electronic systems, both analog and digital. The ability to design communications components such as routers, switches, hubs, transmitters and receivers in different bands.

Learning aims		
Expected results from this subject	Typology	Training and Learning Results
To learn the codesign methods to design applications based on embedded microprocessors in FPGAs.	know	A13 A29 A30
To get to know the microprocessors that can be implemented in commercial FPGAs.	know	A13 A29 A30

To handle the necessary software tools for the development of embedded applications by means of FPGAs.	Know How	A5 A13 A29 A30
To design application specific peripherals and their connection to the buses of the embedded microprocessors.	Know How	A5 A13 A29 A30
To design real applications with embedded microprocessors in FPGAs.	Know How	A5 A6 A13 A29 A30

Contents	
Topic	
LESSON 1 THEORY. INTRODUCTION TO THE DESIGN OF EMBEDDED SYSTEMS. (1 h.)	1.1.- Introduction. 1.2.- Programmable Systems On Chip (PSOC). 1.3.- Hardware / Software Codesign. Codesign phases. 1.4.- Xilinx EDK tool for codesign of embedded systems.
LESSON 2 THEORY. XILINX EMBEDDED MICROPROCESSOR. MICROBLAZE. (0'5 h.)	2.1.- Introduction. 2.2.- Internal architecture of the Microblaze microprocessor. 2.2.1.- Structure of the Microblaze microprocessor. 2.2.2.- Memory Map. 2.2.3.- Buses of the Microblaze microprocessor. LMB, AXI. 2.2.4.- Basic peripherals. Timer. UART RS232. Interrupt Controller. 2.2.5.- Optional Peripherals. Floating Point Unit (FPU).
LESSON 3 THEORY. ARCHITECTURE OF THE XILINX SPARTAN 6 FAMILY OF FPGAs. (0'5 h.)	3.1.- Introduction. 3.2.- Internal Architecture of the Xilinx Spartan 6 FPGAs. 3.2.1.- Logical resources: 3.2.2.- Interconnection Resources. 3.2.3.- Technology. 3.2.4.- Other characteristics.
LESSON 4 THEORY. CONNECTION OF PERIPHERAL CIRCUITS TO THE XILINX MICROBLAZE MICROPROCESSOR. (1 h.)	4.1.- Introduction. 4.2.- Interface for basic peripherals. GPIO. 4.3.- Interface for advanced peripherals. IPIF. 4.4.- Interface for user coprocessors.
LESSON 5 THEORY. SOFTWARE DEVELOPMENT FOR THE XILINX MICROBLAZE MICROPROCESSOR. (1 h.)	5.1.- Introduction. 5.2.- Structure of the routines for handling of peripherals. 5.3.- Interrupt handle. 5.4.- Program debugging.
LESSON 6 THEORY. HARDWARE / SOFTWARE PARTITIONING. (1 h.)	6.1.- Introduction. 6.2.- Examples of hardware / software codesign. 6.3.- Distribution of tasks between hardware and software.
LESSON 7 THEORY. DESIGN PROJECT. DESIGN OF PERIPHERALS FOR XILINX EMBEDDED MICROPROCESSORS. (5 h.)	7.1.- Design of the assigned peripheraL, using the combination of hardware and software which is more suitable.
LESSON 1 LABORATORY. EDK ENVIRONMENT FOR THE DESIGN OF EMBEDDED SYSTEMS BASED IN XILINX 32-BIT MICROPROCESSORS. (2 h.)	1.1.- Introduction. 1.2.- Xilinx EDK (Embedded Development Kit). 1.2.1.- Codesign Flow. 1.2.2.- Wizard for the creation of embedded systems. Base System Builder. 1.2.3.- Addition of predefined peripherals (IP cores). 1.5.- Design of basic examples of embedded systems based in the Microblaze microprocessor. 1.6.- Implementation of the developed systems in Digilent evaluation boards.
LESSON 2 LABORATORY. DESIGN OF BASIC PERIPHERAL CIRCUITS FOR THE XILINX EMBEDDED MICROPROCESSORS. (2 h.)	2.1.- Introduction. 2.2.- Use of predefined peripherals. IPs. 2.2.- Development of basic user peripherals. GPIO.
LESSON 3 LABORATORY. DESIGN OF ADVANCED PERIPHERAL CIRCUITS FOR THE XILINX EMBEDDED MICROPROCESSORS. (2 h.)	3.1.- Introduction. 3.2.- Development of advanced user peripherals. Custom IP. 3.3.- Development of user coprocessors.

LESSON 4 LABORATORY. SDK ENVIRONMENT FOR THE DESIGN OF SOFTWARE FOR THE XILINX 32-BIT MICROPROCESSORS. (2 h.)	4.1.- Introduction. 4.2.- Xilinx SDK. Software Development Kit. 4.2.1.- GNU tools (GCC, ASsembler). 4.2.2.- Editor. Compiler. Linker. 4.2.3.- Supplied Libraries. 4.2.4.- Software analysis. Software profiler. 4.3.- Design Examples. 4.3.1.- Timer handled by interruption.
LESSON 5 LABORATORY. HARDWARE/SOFTWARE VERIFICATION OF EMBEDDED APPLICATIONS. (2 h.)	5.1.- Introduction. 5.2.- Simulation of embedded systems. 5.3.- Debugging of embedded systems by means of the XMD debugger included in SDK 5.4.- Debugging of embedded systems by means of the GNU debugger included in SDK. 5.5.- HW/SW Co-Verification of embedded systems by means of Xilinx Chipscope hardware analyser and the GNU software debugger.
LESSON 6 LABORATORY. DESIGN PROJECT. DESIGN OF AN APPLICATION BASED IN XILINX 32-BIT MICROPROCESSORS. (10 h.: 5 h. Type B + 5 h. Type C)	6.1.- Design and test of the assigned application.

Planning

	Class hours	Hours outside the classroom	Total hours
Master Session	5	10	15
Integrated methodologies	5	20	25
Laboratory practises	10	10	20
Integrated methodologies	9	48	57
Presentations / exhibitions	1	7	8

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies

	Description
Master Session	Conventional lectures. Through this methodology the outcomes CE11/TT11 and CE12/TT12 are developed.
Integrated methodologies	Problem based learning (PBL): Problem solving. Design of synthesisable circuits in VHDL and software programs in C language. To solve them, the student has to previously develop certain outcomes. Through this methodology the outcomes CB5, CG1, CG8, CE11/TT11 and CE12/TT12 are developed.
Laboratory practises	VHDL design of digital circuits and circuit implementation in FPGAs and development of software programs in C language. Integration of both to build an embedded system in a FPGA. Through this methodology the outcomes CB5, CG8, CE11/TT11 and CE12/TT12 are developed.
Integrated methodologies	Project based learning. The students must design an embedded system to solve a problem. In order to that, the students must plan, design and implement the necessary steps. Through this methodology the outcomes CB5, CG1, CG8, CE11/TT11 and CE12/TT12 are developed.
Presentations / exhibitions	Exhibition of the results of the project developed. Through this methodology the outcomes CB5, CG1, CG8, CE11/TT11 and CE12/TT12 are developed.

Personalized attention

Methodologies	Description
Master Session	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.
Presentations / exhibitions	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.
Laboratory practises	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.
Integrated methodologies	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.

Integrated methodologies	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.

Assessment

	Description	Qualification
Integrated methodologies	Problem Based Learning. Resolution of exercises and theoretical problems. The majority of them will be focused on the theoretical approach to the design of a peripheral of an embedded system. The problems will be based on the theoretical topics. It will be necessary to show to the professor the operation of each one of the circuits and programs. The correct application of the theoretical concepts to the problems will be assessed, based on the published criteria. It will be necessary to deliver the documentation requested by the professor for each one of the exercises. Through this methodology the outcomes CB5, CG1, CG8, CE11/TT11 and CE12/TT12 are assessed.	25
Laboratory practises	Design circuits and programs in the laboratory sessions corresponding to the laboratory lessons 1 to 5. It will be necessary to show to the professor the operation of each one of the circuits and programs. It will be necessary to deliver the design source files. The assessment will be based on the operation of the digital system and the correct application of the theoretical concepts, according to the published criteria. Through this methodology the outcomes CB5, CG8, CE11/TT11 and CE12/TT12 are assessed.	25
Integrated methodologies	Project Based Learning. Laboratory Project. Design of an embedded system. It will be necessary to deliver the files source of the work realised. It will be necessary to deliver the design source files. The assessment will be based on the operation of the embedded system and the correct application of the theoretical concepts, according to the published criteria. Through this methodology the outcomes CB5, CG1, CG8, CE11/TT11 and CE12/TT12 are assessed.	40
Presentations / exhibitions	It will be necessary to do an oral presentation of 15 minutes as a maximum about the work, according to the index supplied by the teacher. Through this methodology the outcomes CB5, CG1, CG8, CE11/TT11 and CE12/TT12 are assessed.	10

Other comments on the Evaluation

The total mark will be the sum of the marks obtained in the different tasks of the subject.

The global mark of the theoretical problems has to be equal or greater than 5 over 10 in order to pass the subject.
The mark of the Laboratory Project has to be equal or greater than 5 over 10 in order to pass the subject.

All the students, both those who follow the subject continuously and those who want to be assessed in the final exam at the end of the term or in the extraordinary exam in July, will have to do the tasks described in the previous section.
The students that do not attend classes regularly will also have to do the same tasks as the students who attend classes.

The final mark will be expressed in numerical form ranging from 0 to 10, according to the valid regulation (Royal decree 1125/2003 of 5 September; BOE 18 September).
Following the guidelines of the degree the students will be offered two assessment systems: continuous assessment and final assessment at the end of the term.

CONTINUOUS ASSESSMENT:
 The students are considered to have chosen the continuous assessment when they have done 2 laboratory practices and/or 2 reports of theoretical exercises.
 The students that have chosen continuous assessment, but do not pass the course, will have to do the final assessment in July.
 The students that pass the course by means of continuous assessment will not be allowed to repeat any task in the final assessment in order to improve the mark.
 The different tasks should be delivered in the date specified by the teacher, otherwise they will not be assessed for the

continuous assessment.
 The students will develop the theoretical exercises, the laboratory practices and the laboratory projects in groups of two students during the continuous assessment.
The students who want to be assessed in the continuous assessment can only miss two sessions as a maximum.. If they miss more than 2 sessions, it will be compulsory to do an additional individual task or an examination.

FINAL ASSESSMENT:
 The students that opt for the final assessment will have to do all the theoretical and practical tasks and the project individually.
 The tasks for the final assessment have to be delivered before the official date of the examination set by the faculty.

In case the students pass the theoretical exercises (TE), the laboratory practices (LAB) and the laboratory project (LP), that is, the mark of each part >= 5, the final mark (FM) will be the weighted sum of the marks of each part of the subject:
NF = 0'25 * TE + 0'25 * LAB + 0'40 * LP + 0'10 * OP

In case the students do not pass any of the three main parts of the subject, that is, the mark of any task < 5, the final mark (FM) will be:
NF = Minimum [4'5; (NF = 0'25 * TE + 0'25 * LAB + 0'40 * LP + 0'10 * OP)]

Where:
TE = Global mark of the theoretical exercises and problems.
LAB = Guided Laboratory Practices.
LP = Laboratory Project.
OP = Oral presentation.

ASSESSMENT CRITERIA.
1) Theoretical exercises and problems.
Each one of the theoretical exercises and problems proposed in the theoretical sessions will be marked from 0 to 10. Its influence in the total mark of the subject will be weighted in function of the number of exercises assigned.
The majority of the exercises will consist in the design of a peripheral for an embedded system embedded and the approach to the design of a complete embedded system with its peripherals.
The assessment criteria are the following:

1) Suitable distribution of tasks between hardware and software".

2) Suitable organisation of the hardware and suitable structure of the program in C.

3) Correct design (CORR).
Optimisation of the description in VHDL and the programs in C.
Synchronous design.
Reusable design.

4) Functionality (FUNC). If the exercise asks for it, the behavioural simulation and synthesis of the VHDL, as well as the simulation of the C programs have to work perfectly.

5) Documentation (DOC).
i. Design source files.
ii. Enough comments in the VHDL files and C files to explain the sentences used.

It will be necessary to deliver the required source files.
The total mark will be the sum of the marks of each one of the exercise reports divided by the number of reports:

TE = (Exercise 1 + + Exercise N) / N

2) Realisation of guided laboratory practices.

It will evaluate the correct operation of the circuits and programs developed in the laboratory sessions. Each laboratory lesson will be marked from 0 to 10. Its influence in the total mark of the subject will be weighted in function of the number of hours assigned to each lesson.
That is, the mark of the practices corresponding to the laboratory lessons 1 to 5 will be obtained through the following

formula:

LAB = (Lesson 1L + Lesson 2L + Lesson 3L + Lesson 4L + Lesson 5L) / 5

The total mark of the guided laboratory practices (LAB) will correspond to 25% of the total mark of the subject.
It will be necessary to deliver the required source files.
The assessment criteria refer only to the functionality of the circuits and programs developed, that is, the circuits and programs have to work perfectly to obtain the maximum mark.

3) Laboratory Project.
This project consists in the design of an embedded system.

The assessment criteria are the following:

1) Suitable distribution of tasks between "hardware" and "software".

2) Suitable organisation of the hardware system and suitable structure of the program in C.

3) Correct design (CORR).
System entirely synthesisable.
Suitable hierarchy arrangement.
Design totally synchronous.
Technology independent design.
Reusable design.

4) Analysis of the design and the implementation in FPGAs (ANA).
Analysis of the FPGA logical resources used and their justification.
Analysis of the internal system delays.
Analysis of the chosen implementation options.
Optimal utilisation of the FPGA logical resources.
Achievement of an optimal processing speed.
"Chipscope" Verification.

5) Functionality (FUNC).
Software Simulation.
Software Debugging.
Behavioural and Timing Simulation of the different hardware circuits.
Simulation of the complete embedded system (hardware + software).
Debugging of the complete embedded system (hardware + software).
Board test of the complete embedded system (hardware + software).
All the sections have to work perfectly to obtain the maximum mark.

6) Documentation of the design and the implementation with FPGAs (DOC).
a. Document.
i. Clear structure and order.
ii. Clear and sufficient explanations for the understanding of the work developed.
iii. Include suitable figures.
iv. Include important data.

b. Source design files.
i. Sufficient comments in the VHDL files for its understanding.
ii. Sufficient comments in the C files for its understanding.

For the Laboratory Project (LP), it will be necessary to do an oral presentation.

4) Oral Presentation.

The work developed during the laboratory project will be presented.

The assessment criteria are the following:

1. Clear structure and presentation order.
2. Clear explanations.
3. Enough explanations to understand the project.
4. Suitable figures.
5. Relevant data.

Sources of information

ÁLVAREZ RUIZ DE OJEDA, L.J., POZA GONZÁLEZ, F., **Diseño de aplicaciones empotradas de 32 bits en FPGAs con Xilinx EDK 10.1 para Microblaze y Power-PC**, Vison Libros,

ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño Digital con FPGAs**, Vision Libros,

Recommendations

Subjects that are recommended to be taken simultaneously

(*)Sistemas Electrónicos Dixitais Avanzados/V05M145V03203