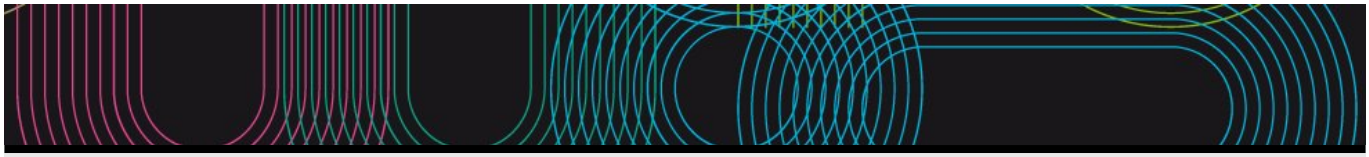

IDENTIFYING DATA				
Advanced Digital Electronic Systems				
Subject	Advanced Digital Electronic Systems			
Code	V05M145V01203			
Study programme	Máster Universitario en Ingeniería de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	5	Mandatory	1st	1st
Teaching language	#EnglishFriendly Spanish			
Department				
Coordinator	Valdés Peña, María Dolores			
Lecturers	Moure Rodríguez, María José Valdés Peña, María Dolores			
E-mail	mvaldes@uvigo.es			
Web	http://moovi.uvigo.gal/course			
General description	The objective of this course is to provide students with the ability to design complex or high frequency digital systems. Firstly, the electrical characteristics, power consumption, speed and fan-out of digital integrated circuits and the technologies of semiconductor memories are studied. Subsequently, the interface with external peripherals and the methodology for designing synchronous sequential systems are analyzed. Finally, the course focuses on the design of digital communications systems implemented using high density integrated programmable circuits. Meanwhile, throughout all contents, emphasis is placed in the VHDL description of high complexity digital systems. English Friendly subject: International students may request from the teachers: a) materials and bibliographic references in English, b) tutoring sessions in English, c) exams and assessments in English.			

Training and Learning Results	
Code	
A4	CB4 Students must communicate their conclusions, and the knowledge and reasons stating them-, to specialists and non-specialists in a clear and unambiguous way.
A5	CB5 Students must have learning skills to allow themselves to continue studying in largely self-directed or autonomous way
B4	CG4 Capacity for mathematical modeling, calculation and simulation in technological centers and engineering companies, particularly in research, development and innovation tasks in all areas related to Telecommunication Engineering and associated multidisciplinary fields.
B8	CG8 Ability to apply acquired knowledge and to solve problems in new or unfamiliar environments within broader and multidiscipline contexts, being able to integrate knowledge.
C10	CE10 Ability to design and manufacture integrated circuits.
C11	CE11 Knowledge of hardware description languages for high complexity circuits.
C12	CE12 Ability to use programmable logic devices, as well as to design advanced electronic systems, both analog and digital. The ability to design communications components such as routers, switches, hubs, transmitters and receivers in different bands.
C14	CE14 Ability to develop electronic instrumentation, as well as transducers, actuators and sensors.

Expected results from this subject	
Expected results from this subject	Training and Learning Results
The knowledge of the integrated circuit manufacturing technologies.	C10
The ability to analyze and design advanced digital circuits.	B4 C12
The knowledge of different input/output technologies of digital circuits.	C14

The ability to design input/output interface circuits.	C10 C12 C14
The knowledge of the design methodologies of complex digital circuits.	A5 B8 C12
The ability to design communication components using programmable logic devices.	A4 B8 C11 C12
The ability to design complex digital electronic systems using hardware description languages.	C11

Contents

Topic	
Introdution to digital integrated circuits	CMOS technology: NMOS and PMOS technologies, CMOS gates, CMOS fabrication. HW design methodologies: custom, semicustom, cell-based, array-based, programmable logic devices (FPGAs). SW design methodologies: abstraction levels, design methods, design flow, IPs.
Advanced VHDL	VHDL description of complex digital systems: variables, arrays, records, generics, generate, funcion, procedure. VHDL coding of Finite State Machines. Advances synthesis: inference, primitives, IPs.
CMOS integrated circuits	Design Metrics: voltages, noise, fan-in, fan-out, delay, power. Power issues in FPGAs Input/Output: standard levels, package. Timing issues: set-up, hold, metastability, skew, jitter, clock distribution.
Sequential design	Synchronizers: asynchronous inputs, PLLs, DLLs Clocking resources in FPGAs. Sequential Design methods: Moore and Mealy Finite State Machines.
Semiconductor memories	Architecture of semiconductor memories: RAM, CAM, ROM, EEPROM, FLASH. Memory Interfacing: RAM, DRAM, EEPROM, FLASH interfacing. Memory in FPGAs: distributed, blocks, external memory, memory IPs.
Arithmetic in FPGAs	Numeric representations. Overflow. Techniques to mitigate overflow. Precision vs. hardware cost. Arithmetic operations. Low cost hardware implementations. Design arithmetic considerations for HDL coding.
Frequency synthesis for communication applications	Frequency synthesis using numerically controlled oscillators (NCOs). NCO architecture. Design parameters. Spurious Free Dynamic Range (SFDR) characterization. Design techniques. NCO implementation using FPGAs.
Retiming and pipeline techniques	Signal flow graphs (SFGs). Analysis of the critical path of digital systems. Analysis of the input to output latency. Retiming techniques to reduce propagation delay in digital systems: pipelining and time scaling. Applying retiming techniques to the design of digital filters. Hardware cost. Applying the concepts to the implementation of digital filters using FPGAs.
Series vs. parallel implementation issues	Design techniques: fully serial, fully parallel, serial-parallel. Hardware cost and timing issues. Applying the concepts to the implementation of digital filters using FPGAs.

Hardware-in-the-loop	Description, simulation and test of FPGAs based circuits. Applying the concepts to the design of data acquisition and signal processing circuits. Using tools for hardware-in-the-loop.
Laboratory Practices	Advanced tools for the design and test of complex digital circuits. Design and implementation of ADC/DAC interfaces, sensor interfaces, digital signal processing modules, communications blocks and memory interfaces.

Planning			
	Class hours	Hours outside the classroom	Total hours
Lecturing	24	17	41
Laboratory practical	10	15	25
Project based learning	5	10	15
Objective questions exam	1	10	11
Problem and/or exercise solving	0	10	10
Laboratory practice	0	5	5
Project	0	18	18
*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.			

Methodologies	
	Description
Lecturing	The professor explains the theoretical contents of the course, encouraging critical discussion and the student involvement. Reading assignments for each session will be previously available via Moovi, and students are expected to come to the theoretical class having completed the assigned reading. Through lecturing sessions the outcomes A5, C10, C11, C12 and C14 are developed.
Laboratory practical	During laboratory sessions students apply the design methods described in the lecturing sessions. All practices are guided and supervised by the professor. Through laboratory practises the outcomes B4, C10, C11, C12 and C14 are developed.
Project based learning	This activity focuses on applying the design techniques studied in the theoretical classes and the skills acquired at the laboratory to a project implementation. Students should obtain well founded solutions, choosing appropriate methods and devices. These projects are planned and tutored in small size groups. Through this activity the outcomes A4, A5, B4, B8, C10, C11, C12 and C14 are developed.

Personalized assistance	
Methodologies	**Description**
Lecturing	Students have the opportunity to resolve doubts in personalized attention sessions. The appointment with the corresponding professor must be requested and agreed by email, preferably within the hours published on the faculty website. The links to the contact details of the teachers are: María José Moure Rodríguez - https://moovi.uvigo.gal/user/profile.php?id=11642 María Dolores Valdés Peña - https://moovi.uvigo.gal/user/profile.php?id=11303
Laboratory practical	Students have the opportunity to resolve doubts in personalized attention sessions. The appointment with the corresponding professor must be requested and agreed by email, preferably within the hours published on the faculty website. The links to the contact details of the teachers are: María José Moure Rodríguez - https://moovi.uvigo.gal/user/profile.php?id=11642 María Dolores Valdés Peña - https://moovi.uvigo.gal/user/profile.php?id=11303
Project based learning	Meetings will be planned with each student team to supervise the progress of the projects.
Tests	**Description**
Problem and/or exercise solving	Students have the opportunity to resolve doubts in personalized attention sessions. The appointment with the corresponding professor must be requested and agreed by email, preferably within the hours published on the faculty website. The links to the contact details of the teachers are: María José Moure Rodríguez - https://moovi.uvigo.gal/user/profile.php?id=11642 María Dolores Valdés Peña - https://moovi.uvigo.gal/user/profile.php?id=11303

Assessment

	Description	Qualification	Training and Learning Results
Objective questions exam	At the end of the semester there will be an exam of short problems and/or development questions. This exam asses all of the contents taught in the theoretical classes.	30	C10 C11 C12 C14
Problem and/or exercise solving	Students will solve a set of problems and/or system design exercises. It represents 10% of the final score.	10	C10 C11 C12 C14
Laboratory practice	The assessment of the laboratory practices takes place during the practical sessions. The student should complete at least 4 of the 5 sessions. The implementation of the circuits described in the practice guidelines and the reports submitted at the end on each session will deserve the 30% of the final grade.	30	B4 C10 B8 C11 C12 C14
Project	Students will develop a design project in groups of 2 persons, preferably, demonstrating the skills acquired in the theoretical lessons and laboraory practices. The project represents the 30% of the final grade.	30	A5 B4 C10 B8 C11 C12 C14

Other comments on the Evaluation

The subject can be passed with the maximum grade through continuous assessment (CA) or global assessment (GA). Both evaluation methods are mutually exclusive. The student who attends more than 2 laboratory sessions is considered to have opted for continuous assessment. However, those who wish to waive continuous assessment may do so within a maximum period of one month before the end of the semester.

1. Continuous assessment:

Students who opt for the CA modality will have two evaluation opportunities, the ordinary call at the end of the semester and the extraordinary one at the end of the course (June-July).

1.1 Ordinary call

The ordinary call consists of a set of assessments that will be carried out throughout the semester. The dates of all the tests will be published in a shared calendar and will be available at the beginning of the semester.

The weight and content of the assesssments is as follows:

- Objective questions exam and/or questions of development (NExam):

- It covers all of the contents taught in the theoretical classes. Includes short problems or questions, or multiple answer questions.
- The exam will last 1 hour (type A hour).
- The student passes this part if he/she gets a mark greater than or equal to 4 over 10.

- Problem and/or exercise solving (NExerc):

- It consists of a set of problems and/or design exercises that students must solve and deliver on certain previously stipulated dates.
- These activities would be realized outside the classroom hours.
- The student passes this part if he/she gets a mark greater than or equal to 4 over 10.

- Laboratory practices (NPrac):

- The student must correctly implement the circuits described in the practice scripts and deliver a results report corresponding to each practice. The mark of each practice depends on these results.
- It can be done individually or by groups of 2 students. In the latter case, if both attend the practice, the mark is the same for both.
- The practices are compulsory. The students must attend at least 4 of the 5 practice sessions (80% compulsory attendance).

- Project (NPro):

- It must be done by collaborative groups of 2 students, preferably.
- This project will be carried out in type C hours under the supervision of the responsible faculty.
- The student passes this part if they obtain an NPro grade greater than or equal to 4 out of 10.

Continuous assessment final grade (Final_CA):

The final grade of the ordinary CA is obtained as follows:

Final_CA = (NExam*0.3 + NExerc*0.1 + NPrac*0.3 + NPro*0.3) if NExam, NExerc and NPro are greater than or equal to 4;

Final_CA = min [(NExam*0.3 + NExerc*0.1 + NPrac*0.3 + NPro*0.3), 4.9] in any other case;

1.2 Extraordinary call:

The student that does not pass one or more assessments of the ordinary call can recover the following parts in the extraordinary call:

- He/she can complete the project and this mark replaces the previous one (NPro).
- He/she can take the theoretical exam and this mark replaces the previous one (NExam).
- He/she can do the problems and/or design exercises and this mark replaces the previous one (NExerc).

The final grade of the extraordinary call is obtained in the same way as the ordinary one.

2. Global assessment:

As with the continuous assessment, students who opt for global assessment will have two opportunities, ordinary and extraordinary calls. In both cases it will consist of the following parts:An exam in which all the theoretical contents of the subject are evaluated. It consists of several short problems and/or development questions and lasts 2 hours. To pass the subject it is necessary to obtain a 4 out of 10. This exam
represents 40% of the final grade (NExam).

- A practical exam covering the same aims of the labortory practices developed during the course. This exam lasts 2 hours. The weight of this evaluation represents 20% of the final grade (Nprac).

- An individual project with the same objectives and complexity as the project carried out in the continuous assessment. This project represents 40% of the final grade (NPro). To pass the subject it is necessary to obtain a grade greater than or equal to 4 out of 10.

Global assessment final grade (Final_GA):

The final grade (Final_GA) is obtained as follows:Final_GA = (NExam*0.4 + NPrac*0.2 + NPro*0.4) if NExam and NPro are greater than or equal to 4;Final_GA = min [(NExam*0.4 + NPrac*0.2 + NPro*0.4), 4.9] in any other case.

3. Other comments:

- Students may write their reports, papers, exams or presentations in Spanish, Galician or English.
- The grades obtained in the continuous or global assessment are only valid for the current academic year.
- The use of books, notes or electronic devices such as phones or computers is not permitted in any exam. Mobile phones must be turned off and out of reach of the student.
- Plagiarism is regarded as serious dishonest behavior. In the case that plagiarism is detected in any of the reports/tasks/exams done/taken, the final grade will be FAIL (0), and the incident will be reported to the corresponding academic authorities for prosecution.

Sources of information

Basic Bibliography

Complementary Bibliography

Weste N., Harris D., **CMOS VLSI Design. A circuits and systems perspective**, 4, 2011

Roth C.H., John L.K., **Digital systems design using VHDL**, 3, 2008

Sharma A.K., **Semiconductor memories : technology, testing, and reliability**, 1997

Kurinec S.K., Iniewski K., **Nanoscale Semiconductor Memories: Technology and Applications (Devices, Circuits, and Systems)**, 2013

Kleitz W., **Digital Electronics: A Practical Approach with VHDL**, 9, 2011

Comer D.J., **Digital logic and state machine design**, 3, 1995

Wakerly J.F., **Digital Design. Principles and Practices**, 4, 2007

Moure M.J., Valdés M.D:, **Apuntes y prácticas de SEDA**, 2017

Recommendations

Subjects that are recommended to be taken simultaneously

Digital and Analog Mixed Circuits/V05M145V01213
Hardware/Software Design of Embedded Systems/V05M145V01214