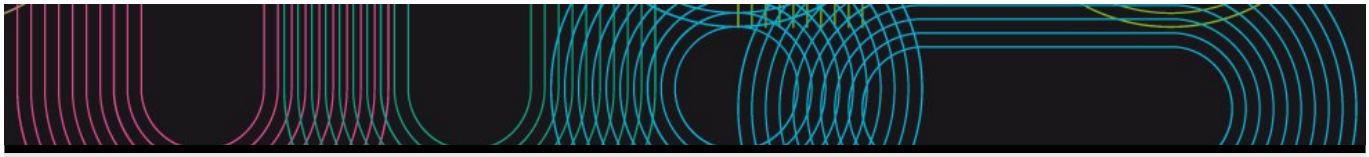

IDENTIFYING DATA				
Advanced Digital Electronic Systems				
Subject	Advanced Digital Electronic Systems			
Code	V05M145V01203			
Study programme	Telecommunication Engineering			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	5	Mandatory	1st	2nd
Teaching language	Spanish			
Department				
Coordinator	Valdés Peña, María Dolores			
Lecturers	Moure Rodríguez, María José Valdés Peña, María Dolores			
E-mail	mvaldes@uvigo.es			
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General description	The objective of this course is to provide students with the ability to design complex or high frequency digital systems. Firstly, the electrical characteristics, power consumption, speed and fan-out of digital integrated circuits and the technologies of semiconductor memories are studied. Subsequently, the interface with external peripherals and the methodology for designing synchronous sequential systems are analyzed. Finally, the course focuses on the design of digital communications systems implemented using high density of integration programmable circuits. Meanwhile, throughout all contents, emphasis is placed in the VHDL description of high complexity digital systems.			

Competencies	
Code	
A4	CB4 Students must communicate their conclusions, and the knowledge and reasons stating them-, to specialists and non-specialists in a clear and unambiguous way.
A5	CB5 Students must have learning skills to allow themselves to continue studying in largely self-directed or autonomous way
B4	CG4 Capacity for mathematical modeling, calculation and simulation in technological centers and engineering companies, particularly in research, development and innovation tasks in all areas related to Telecommunication Engineering and associated multidisciplinary fields.
B8	CG8 Ability to apply acquired knowledge and to solve problems in new or unfamiliar environments within broader and multidiscipline contexts, being able to integrate knowledge.
C10	CE10 Ability to design and manufacture integrated circuits.
C11	CE11 Knowledge of hardware description languages for high complexity circuits.
C12	CE12 Ability to use programmable logic devices, as well as to design advanced electronic systems, both analog and digital. The ability to design communications components such as routers, switches, hubs, transmitters and receivers in different bands.
C14	CE14 Ability to develop electronic instrumentation, as well as transducers, actuators and sensors.

Learning outcomes	
Expected results from this subject	Training and Learning Results
The knowledge of the different technologies of integrated circuits manufacture.	C10
The ability to analyze and design advanced digital circuits.	B4 C12
The knowledge of different input/output technologies of digital circuits.	C14
The ability to design input/output interface circuits.	C10 C12 C14
The knowledge of the methodologies for the design of complex digital circuits.	A5 B8 C12

The ability to design communication components using programmable logic devices.	A4 B8 C11 C12
The ability to design complex digital electronic systems using hardware description languages.	C11

Contents

Topic	
Introdution to digital integrated circuits	CMOS technology: NMOS and PMOS technologies, CMOS gates, CMOS fabrication. HW design methodologies: custom, semicustom, cell-based, array-based, programmable logic devices (FPGAs). SW design methodologies: abstraction levels, design methods, design flow, IPs.
Advanced VHDL	VHDL description of complex digital systems: variables, arrays, records, generics, generate, funcion, procedure. VHDL coding of Finite State Machines. Advances synthesis: inference, primitives, IPs.
CMOS integrated circuits	Design Metrics: voltages, noise, fan-in, fan-out, delay, power. Power issues in FPGAs Input/Output: standard levels, package. Timing issues: set-up, hold, metastability, skew, jitter, clock distribution.
Sequential design	Synchronizers: asynchronous inputs, PLLs, DLLs Clocking resources in FPGAs. Sequential Design methods: Moore and Mealy Finite State Machines.
Semiconductor memories	Architecture of semiconductor memories: RAM, CAM, ROM, EEPROM, FLASH. Memory Interfacing: RAM, DRAM, EEPROM, FLASH interfacing. Memory in FPGAs: distributed, blocks, external memory, memory IPs.
Arithmetic in FPGAs	Numeric representations. Overflow. Techniques to mitigate overflow. Precision vs. hardware cost. Arithmetic operations. Low cost hardware implementations. Design arithmetic considerations for HDL coding.
Frequency synthesis for communication applications	Frequency synthesis using numerically controlled oscillators (NCOs). NCO architecture. Design parameters. Spurious Free Dynamic Range (SFDR) characterization. Design techniques. NCO implementation using FPGAs.
Retiming and pipeline techniques	Signal flow graphs (SFGs). Analysis of the critical path of digital systems. Analysis of the input to output latency. Retiming techniques to reduce propagation delay in digital systems: pipelining and time scaling. Applying retiming techniques to the design of digital filters. Hardware cost. Applying the concepts to the implementation of digital filters using FPGAs.
Series vs. parallel implementation issues	Design techniques: fully serial, fully parallel, serial-parallel. Hardware cost and timing issues. Applying the concepts to the implementation of digital filters using FPGAs.
Hardware-in-the-loop	Description, simulation and test of FPGAs based circuits using Matlab/Simulink. Applying the concepts to the design of data acquisition and signal processing circuits. Using tools for hardware-in-the-loop.

Laboratory Practices	Advanced tools for the design and test of complex digital circuits. Design and implementation of ADC/DAC interfaces, sensor interfaces, digital signal processing modules, communications blocks and memory interfaces.

Planning			
	Class hours	Hours outside the classroom	Total hours
Lecturing	22	15	37
Laboratory practical	10	15	25
Project based learning	5	10	15
Objective questions exam	1	10	11
Problem and/or exercise solving	0	10	10
Laboratory practice	0	5	5
Project	0	18	18
Presentation	2	2	4
*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.			

Methodologies	
	Description
Lecturing	The professor explains the theoretical contents of the course, encouraging critical discussion and the student involvement. Reading assignments for each session will be previously available via FaiTIC, and students are expected to come to the theoretical class having completed the assigned reading. Through master sessions the outcomes CB5, CE10, CE11, CE12 and CE14 are developed.
Laboratory practical	During laboratory sessions students apply the design methods described in the master sessions. All the sessions are guided and supervised by the professor. Through laboratory practises the outcomes CG4, CE10, CE11, CE12 and CE14 are developed.
Project based learning	This activity focuses on applying the techniques described in the lecture classes and the skills developed at laboratory to a project implementation. Students should obtain well founded solutions, choosing appropriate methods and devices. These projects are planned and tutored in small size groups. Through master sessions the outcomes CB4, CB5, CG4, CG8, CE10, CE11, CE12 and CE14 are developed.

Personalized assistance	
Methodologies	**Description**
Lecturing	Students have the opportunity to solve doubts in personalized attention sessions. The appointment with the corresponding professor should be required and agreed by e-mail, preferably in the hours which are published in the faculty website.
Laboratory practical	Students have the opportunity to solve doubts in personalized attention sessions. The appointment with the corresponding professor should be required and agreed by e-mail, preferably in the hours which are published in the faculty website.
Project based learning	Meetings will be planned with each group of students to supervise the progress of the projects.
Tests	**Description**
Problem and/or exercise solving	Students have the opportunity to solve doubts in personalized attention sessions. The appointment with the corresponding professor should be required and agreed by e-mail, preferably in the hours which are published in the faculty website

Assessment			
	Description	Qualification	Training and Learning Results
Objective questions exam	A questions of development type exam will be done at the end of the term. This exam asses all of the contents taught in the theoretical classes.	20	C10 C11 C12 C14

Problem and/or exercise solving	Students will solve a set of problems and/or system design exercises. It represents 10% of the final score.	10			C10 C11 C12 C14
Laboratory practice	This evaluation takes place during the practical sessions. The student should complete at least 4 of the 5 sessions. The implementation of the circuits described in the practice guidelines and the reports submitted at the end on each session will deserve the 30% of the final qualification.	30		B4 B8	C10 C11 C12 C14
Project	The students will develop a design project in groups of 4 or more persons, preferably, demonstrating the skills acquired in the master lessons and laboraory practices. The project represents the 35% of the final grade.	35	A5	B4 B8	C10 C11 C12 C14
Presentation	At the end of the term students must present the results of their pojects both written and orallly. This activity represents 5% of the final grade.	5	A4		

Other comments on the Evaluation

A pass mark can be achieved in the subject either by continuous evaluation or single evaluation. Both evaluation methods are excluding. Students who assist to more than 2 laboratory sessions are graded using continuous evaluation.

1. Continuous evaluation

Students who opt for the continuous evaluation method will have two assessment opportunities, a first call at the end of the term and a second call at the end of the course (June July).

The first call consists of four different evaluation activities that will be carried out throughout the term. The dates of all evaluations will be published at the beginning of the term. The weighting and content of each continuous assessment part are as follows:

1.1 Objective questions exam and/or questions of development (NExam):

- It covers all of the contents taught in the theoretical classes. Includes short problems or questions, or multiple answer questions.
- The exam will last 1 hour (type A hour).
- The student passes this part if he/she gets a mark greater than or equal to 4 over 10.

1.2 Problem and/or exercise solving (NExerc):

- It consists of a set of problems and/or design exercises that students must solve and deliver on certain previously stipulated dates.
- These activities would be realized outside the classroom hours.
- The student passes this part if he/she gets a mark greater than or equal to 4 over 10.

1.3 Laboratory practices (NPrac):

- The student should correctly implement the circuits described in the guidelines of the practice and submit a report corresponding to each laboratory session. The qualification of each practice depends on these achievements.
- It can be developed individually or by groups of 2 students. In this last case and if both attend the practice, the qualification is the same for the 2 students.

1.4 Project (NPro):

- It should be carried out by collaborative groups of 3 or more students, preferably.
- The 70% of the final mark (NPro) is obtained from the individual tasks assigned to each student and the 30% from the global tasks of the group.
- As part of the individual tasks, each student will be assigned a theoretical work at the begining of the term. This work consists of a preliminary study of the tasks to be carried out in the project. This previous work represents 5% of the final grade of the project.
- In case of plagiarism or abandonment of a member of a work group is detected, his/her score will be fail (0) and will not compute for the score of the rest of the group.
- The student will pass this part if he/she gets an NPro mark greater than or equal to 4 over 10.

1.5 Presentation of the project results (PPro)

Each student must present the results of the project orally and/or in writing. These activities represent 5% of the final grade of the subject.

1.6 Final qualification of continuous evaluation (Final_ac)

The final qualification (Final_ac) of continuous assessment is obtained as follows:

Final_ac = (NExam*0.2 + NExerc*0.1 + NPrac*0.3 + NPro*0.35 + PPro*0.05) if NExam and Npro are greater than or equal to 4;

Final_ca = min [(NExam*0.2 + NExerc*0.1 + NPrac*0.3 + NPro*0.35 + PPro*0.05), 4] in other case;

The student who fails one or more assessments of the continuous evaluation in the first call can recover the following parts in the second call:

- He/she can take the theoretical exam and this mark replaces the previous one (NExam).
- He/she can complete and present his/her project again and these marks replace the previous ones (NPro and PPro).
- He/she can repeat the problems and / or systems design exercises and this mark replaces the previous one (NExerc).

2. Single evaluation

As with continuous evaluation, students who opt for a single evaluation method will have two assessment opportunities, first call and second call. In both cases the single evaluation will consist of the following parts:

- An exam evaluating all the theoretical contents of the subject. It usually consists of several questions of development and short problems and lasts 2 hours. The pass mark for this exam is 4 out of 10 and deserves 40% of the final qualification (NExam).
- A practical exam covering the same aims of the labortory practices developed in continuous evaluation. This exam lasts 2 hours and represents 20% of the final qualification (NPrac).
- An individual project with the same objectives and complexity of the project developed in continuous evaluation. This project deserves 40% of the final qualification (NPro). It is necessary to obtain a mark greater o equal to 4 out of 10 in order to pass the course.

In the case of single evaluation, the final grade (Final_au) is obtained as follows:

Final_au = (NExam*0.4 + NPrac*0.2 + NPro*0.4) if NExam and Npro are greater than or equal to 4;

Final_au = min [(NExam*0.4 + NPrac*0.2 + NPro*0.4), 4] in any other case;

3. Other comments

- The student can use the Spanish, English or Galician for the reports, works, exams or presentations.
- The grades obtained from the continuous or single evaluation are only valid for the current academic year.
- The use of books, notes or electronic devices such as phones or computers is not permitted in any examination. Mobile phones must be turned off and be out of reach of the student.
- In the case that plagiarism is detected in any of the reports/tasks/exams done/taken, the final score for the subject will be fail (0) and the teachers will inform the School authorities so that they take the actions they consider appropriate.

Sources of information
Basic Bibliography
Complementary Bibliography
Weste N., Harris D., **CMOS VLSI Design. A circuits and systems perspective**, 4, 2011
Roth C.H., John L.K., **Digital systems design using VHDL**, 3, 2008
Sharma A.K., **Semiconductor memories : technology, testing, and reliability**, 1997
Kurinec S.K., Iniewski K., **Nanoscale Semiconductor Memories: Technology and Applications (Devices, Circuits, and Systems)**, 2013
Kleitz W., **Digital Electronics: A Practical Approach with VHDL**, 9, 2011
Comer D.J., **Digital logic and state machine design**, 3, 1995
Wakerly J.F., **Digital Design. Principles and Practices**, 4, 2007

Recommendations

Subjects that are recommended to be taken simultaneously

Digital and Analog Mixed Circuits/V05M145V01213
Hardware/Software Design of Embedded Systems/V05M145V01214

Contingency plan

Description

In cases of distance or blended learning all the teaching activities will be carried out using the Remote Campus tool together with the support of the FaiTic platform and email. Besides, the following aspects will be taken into account:

* Lecturing (type A hours):

The theoretical contents of the subject will be remotely taught using the "Campus Remoto" platform.

* Laboratory practices and Project based learning (type B and C hours):

The laboratory practices that can be not developed in the specialized laboratories at the University will be replaced by one or more of the following alternatives:

- Demonstration practices in which the students must attend to them and participate remotely.
- Simulation practices that the students must develop and submit results reports.
- Practices developed with electronic circuits that the students can assembly at home and submit a results report.

The project will be replaced by a theoretical and/or experimental work related to the contents of the subject maintaining its weight in the final grade. In this case, it can be done individually or in groups of 2 students according to the its characteristics and/or its length. The work and guidelines will be published by the teaching staff well in advance.

* Assessment:

The assessment criteria will be the same as in case of classroom or face-to-face teaching.