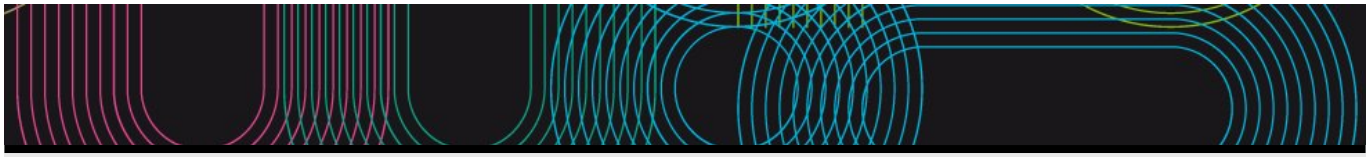

IDENTIFYING DATA				
Integrated Circuits Design and Manufacturing				
Subject	Integrated Circuits Design and Manufacturing			
Code	V05M145V01215			
Study programme	Telecommunication Engineering			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	5	Optional	1st	2nd
Teaching language	Spanish			
Department				
Coordinator	Fariña Rodríguez, José			
Lecturers	Cao Paz, Ana María Fariña Rodríguez, José			
E-mail	jfarina@uvigo.es			
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General description	The objectives in mind are: 1) To know and understand the design methodologies of Integrated Circuits (ICs) based on CMOS technology. 2) To know the basic topologies used in analog electronic circuits. 3) To know how to analyze and dimensioning the devices of the basic topologies of analog circuits in CMOS technology. 4) To know and be capable to use software tools for the design of integrated circuits. 5) To know to specify an integrated circuit for manufacturing in CMOS technology.			

Competencies	
Code	
A4	CB4 Students must communicate their conclusions, and the knowledge and reasons stating them-, to specialists and non-specialists in a clear and unambiguous way.
A5	CB5 Students must have learning skills to allow themselves to continue studying in largely self-directed or autonomous way
B8	CG8 Ability to apply acquired knowledge and to solve problems in new or unfamiliar environments within broader and multidiscipline contexts, being able to integrate knowledge.
C10	CE10 Ability to design and manufacture integrated circuits.

Learning outcomes	
Expected results from this subject	Training and Learning Results
Know the design methodologies of electronic integrated circuits	C10
Know the basic topologies used in analog electronic circuits	C10
Can analyze and dimension the devices that form the basic topologies of analog circuits	A5 B8 C10
Know aid software tools integrated circuit design	C10
Know how an electronic circuit is specified for manufacturing	A4 C10

Contents	
Topic	
Chapter 1: Introduction (1h)	Course introduction. Objectives and course planning. Basic concepts of microelectronic design of integrated circuits (ICs).

Chapter 2: Manufacturing sequence for ICs (1h)	Introduction to ICs manufacturing. Planar technology. Manufacturing sequence of ICs in CMOS technology. Structure of MOS transistors. Manufacturing example: CMOS inverter. Masks pattern (layout). Technological design rules. Methodologies and tools for design assistance.
Chapter 3: Physical structure of basic devices and routing strategies (1h)	Specification of the physical structure of MOS transistor. Specification of the physical structure of a resistor. Specification of the physical structure of a capacitor. Strategies for performing transistors with high aspect ratio. Strategies for matched transistors.
Chapter 4: Basic amplifier topologies (2h)	Common source topology. Common drain topology. Common gate topology. Cascode topology. Push_Pull amplifier. Physical design examples.
Chapter 5: Current mirror (3h)	Current sources. Basic structure of a current mirror. Analysis of functioning. Frequency response. Cascode topology. Physical design examples.
Chapter 6: Differential pair (3h)	Differential pair structure. DC analysis. AC analysis. Specifications and design of the physical structure of a self-biased differential amplifier topology. Common mode rejection ratio. Matching of transistors. Slew rate limitations. Physical design examples.
Chapter 7: Operational amplifier (2h)	Two stages operational amplifier. Design parameters. Operational Transconductance Amplifier (OTA). Examples of physical designs.
Chapter 8: Preparing for manufacturing (2h)	Distribution in the base plane. Pad and terminals. Specification formats. Packages.
Laboratory session 1: Introduction to design tools for ICs (2h)	Introduction to design tools for analog ICs. Current mirror example. Electric simulation. Design Rules Check (DRC) and layout extraction.
Laboratory session 2: Design of self-biased differential pair (2h)	Electrical specification. Characterization of DC operating parameters. Characterization of AC operating parameters.
Laboratory session 3: Design of self-biased differential pair II (2h)	DRC and layout extraction. Layout versus schematic (LVS). Post-layout simulation.
Laboratory session 4: Design of a transconductance amplifier (2h)	Electrical Specification. Physical specification. Operation testing.
Laboratory session 5: Preparing for manufacturing (2h)	For the circuit obtained in Laboratory session 4, perform the required steps to create the information needed in order to send the circuit to manufacture.

Planning

	Class hours	Hours outside the classroom	Total hours
Lecturing	13	26	39
Mentored work	4	28	32
Laboratory practical	9	22.5	31.5
Problem and/or exercise solving	1	3	4
Problem and/or exercise solving	1	3	4
Laboratory practice	1	7	8
Essay	1	5.5	6.5

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies

	Description
Lecturing	The professor will present the relevant concepts of the course. Before each lecture, students must carry out a preparation analysis of the topics to be addressed. The aim is to encourage active participation of students, who may ask questions or expose doubts during the session. For a better understanding of certain content, practical examples or case studies will be discussed
Mentored work	Students will work in small teams (C-type groups) in the physical design and characterization of a circuit consisting of active devices and passive components, under the close guidance of professors. Attendance will be recorded. The activities to be developed by each team are: - Analysis of possible solutions and design alternatives.
Laboratory practical	Students work in groups of two people. They will work with IC CAD tools for IC design, in which they will carried out the definition of an electronic circuit both electrical and physical level, the verification of compliance with specifications and design preparation for manufacturing. Attendance will be recorded and performance of each group in each lab assignment will be evaluated.

Personalized assistance

Methodologies	Description

Lecturing	The teaching staff will attend doubts and enquiries of the students about the theoretical contents, previous preparation of laboratory practices as well as its contents. Professors will also resolve the doubts and enquiries of students about specifications, theoretical and practical aspects of the assigned project as well as those about the content and structure of the explanatory report. In addition, students will be guided about the structure and contents of the sessions of presentation and defense of the results achieved in the project. Students will have the opportunity to attend personalized or group mentoring.
Laboratory practical	The teaching staff will attend doubts and enquiries of the students about the theoretical contents, previous preparation of laboratory practices as well as its contents. Professors will also resolve the doubts and enquiries of students about specifications, theoretical and practical aspects of the assigned project as well as those about the content and structure of the explanatory report. In addition, students will be guided about the structure and contents of the sessions of presentation and defense of the results achieved in the project. Students will have the opportunity to attend personalized or group mentoring.
Mentored work	The teaching staff will attend doubts and enquiries of the students about the theoretical contents, previous preparation of laboratory practices as well as its contents. Professors will also resolve the doubts and enquiries of students about specifications, theoretical and practical aspects of the assigned project as well as those about the content and structure of the explanatory report. In addition, students will be guided about the structure and contents of the sessions of presentation and defense of the results achieved in the project. Students will have the opportunity to attend personalized or group mentoring.

Assessment

	Description	Qualification	Training and Learning Results	
Problem and/or exercise solving	As part of the continuous evaluation, it will take place in mid-course an individual written test of 30 minutes, in one of the lecture sessions. This test will involve 10% of the final grade. This test is the last chance for students to decide whether or not they opt for continuous evaluation. All students completing the test implicitly choose to follow continuous evaluation. The remaining students have to explicitly declare their choice. The lack of declaration from a student means he/she will not follow continuous evaluation. Another written test of 60 minutes will be held in the date of the final exam. This test will have two parts and it is compulsory in whole for students not in continuous evaluation. Students in continuous evaluation can also voluntarily complete the first part since the contents correspond to the first written test. In that case, the score they will receive in this part of the course evaluation will be the one achieved in this second test. The second part of the test is mandatory for all students. Each of the parts will involve 10 % of the final qualification. To pass the course, students must achieve in each part a mark of 4 or higher in a 0-10 scale (or in the intermediate test, where appropriate). Competences CE10 and CB4 will be assessed in these tests.	10	A4	C10
Problem and/or exercise solving	At the end of the theoretical content, students will have a second 60-minute exam, during one of the lectures. This test will represent 10% of the final grade. On the date of the final exam there will be another one-hour written test of this kind, compulsory in its entirety for students who do not opt for continuous evaluation. For students in continuous assessment, it will be voluntary, since the contents correspond to those of the second test. Students who voluntarily present themselves will be substituted for the second test grade for which they obtain in this part. The mark of this exam will be 10% of the final grade. To pass the subject it will be necessary to obtain at least a score of 4 out of 10 in each of the parts of the final test (or in the intermediate test, when appropriate). In this test the competences CE10, CB4 and CG8 are evaluated.	10	A4	C10
Laboratory practice	As part of the continuous assessment of the subject, each student will be evaluated for each of the practices. In the evaluation will take into account the work of preparation prior to the realization of the practice, assistance, punctuality and use. The previous work will have a maximum weight of 30% of the practice grade. The total qualification of the practices will be obtained as an arithmetic average of the qualification of each of them. To be able to make the average, it is necessary to obtain in each practice a grade equal to or greater than 30% of the maximum score of the practice. For justified reasons you can stop doing one of the practices. The note corresponding to this practice will be zero (0.0). If the criterion of the mean can not be applied, the mark of this part will be calculated multiplying by 0.42 the note obtained with the weighted average and it will not be compensable with the theory mark. The internship note is not kept for successive academic courses.In this test the CE10, CB4, CB5 and CG8 skills are evaluated.	20	A4 A5	B8 C10

Essay	The evaluation of the work will be performed from memory supporting and public presentation of results. Each group of students you must submit a report of the work has been carried out, indicating expresses the contribution of each to the whole, as well as methodology followed for the distribution and coordination of tasks. The evaluation of the work will be based on the following aspects: - Analysis of alternatives - Correct implementation and design verification - Design compaction - Use of appropriate strategies to minimize the effects of imperfections in the manufacturing process and to ensure good matching of the electrical characteristics between components or devices that like this require it by functional reasons. - Information for integrated circuit manufacturing. - Formal aspects: clarity and order, including figures and appropriate and outstanding data, as well as explanations in a concrete and comprehensive way. Each student will have an individual public exposure of the project has personally performed (including tasks planning and coordination if applicable). The presentations of the students from each group will be out in the same session, 1 hour. Each student will have 5 minutes for their presentation. At the end of the presentation, students must answer questions from teachers and other students present. The evaluation will be based on both the content and formal aspects of the presentation and the answers to questions. It may also assess positively to students who perform relevant questions. The explanatory report should be submitted at least two days before public presentation of work. To pass the course, the student will need obtain at least a score of 5 over 10 in memory, get to least a score of 5 out of 10 in public presentation. In the evaluation of the practical tests, the memory note will weigh 70% and the presentation 30%. In this test the CE10, CB4, CB5 and CG8 skills are evaluated.	60	A4 B8 C10

Other comments on the Evaluation

- Final test will be 50% of the overall grade of the course. It will consist of two parts: short answer questions and resolution of problems. The part of the questions will represent 40 % of the test qualification and the part of resolution of problems the other 60%. In order to calculate the grade it is necessary to obtain at least 50 % of the maximum score for each part.
- They must develop a project, and deliver the corresponding report and public presentation (in the same sessions and with the same criteria as students in continuous evaluation). Reports are due two days before the public presentation. The project qualification will involve 50% of the overall grade of the course. In the final qualification of the project, the memory report has a corresponding percentage of 70% and the other 30% is obtained from the qualification of the presentation. In order to calculate the grade it is necessary to obtain at least 50 % of the maximum score for each part.

Students not passing the course in the first call will have the opportunity to attend a second call. To pass the course, students must achieve in each part at least 50 % of the maximum score.

Sources of information

Basic Bibliography

R. Jacob Baker, **CMOS Circuits desing, Layout and Simulation**, 978-0-470-88132-3, 3º, John Wiley and Sons, 2010

Paul R. Gray, Paul J. Hurst, Stephen H. Lewis, Robert G. Meyer, **Analysis and Design of Analog Integrated Circuits**, 978-0-470-39877-7, 5º, John Wiley and Sons, 2010

Behzad Razavi, **Design of Analog CMOS Integrated Circuits**, 978-0-07-252493-2, 2º, McGraw Hill, 2017

Stephen A. Campbell, **Fabrication Engineering at the micro-and nanoscale**, 978-0-19-986122-4, 4º, Oxford University Press, 2012

Complementary Bibliography

Recommendations

Contingency plan

Description

=== EXCEPTIONAL PLANNING ===

Given the uncertain and unpredictable evolution of the health alert caused by COVID-19, the University of Vigo establishes an extraordinary planning that will be activated when the administrations and the institution itself determine it, considering safety, health and responsibility criteria both in distance and blended learning. These already planned measures guarantee, at the required time, the development of teaching in a more agile and effective way, as it is known in advance (or well in

advance) by the students and teachers through the standardized tool.

=== ADAPTATION OF THE METHODOLOGIES ===
A the same as in the situation of presence, the delivery of classroom teaching will be based on documentation and other teaching resources that team teaching available to students on the platform teleteaching University and the basic literature available in library. In practice, the same environment design, simulation and testing of integrated circuits in open access versions will be used. Theoretical and practical classes and tutorials will be taught through the remote campus of the University.

=== ADAPTATION OF THE TESTS ===
Evaluation methods and their weights are maintained and, in the case of objective evidence, they will be synchronously remotely using the tools available on campus and remote platform teleteaching.