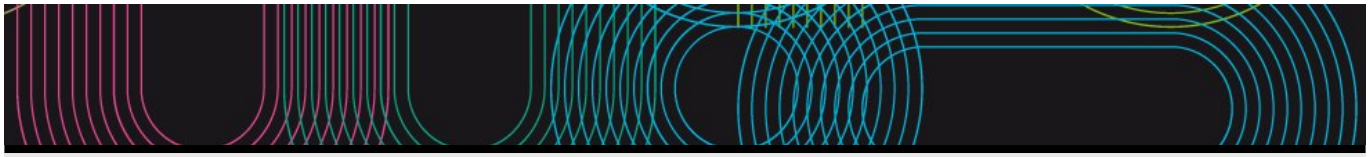
Universidade Vigo

Subject Guide 2023 / 2024



IDENTIFYING DATA				
Digital electronics				
Subject	Digital electronics			
Code	V05G306V01203			
Study programme	Grado en Ingeniería de Tecnologías de Telecomunicación (docencia en inglés)			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Mandatory	2nd	1st
Teaching language	English			
Department				
Coordinator	Pérez López, Serafín Alfonso			
Lecturers	Pérez López, Serafín Alfonso			
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General description	This course is an introduction to the basic principles of digital design and the analysis and design of digital circuits and systems. First, logic circuits, basic digital devices and logic gates representation will be introduced. Then, hardware description languages (HDL) based design, description and simulation methods will be described. Combinational and sequential logic design will be explained using the top-down design paradigm. Finally, the common combinational and sequential logic circuits will be described: operation, diagrams, symbols and VHDL description and simulation.			

Training and Learning Results	
Code	
B13	CG13 The ability to use software tools that support problem solving in engineering.
B14	CG14 The ability to use software tools to search for information or bibliographical resources.
C14	CE14/T9: The ability to analyze and design combinatory and sequential, synchronous and asynchronous circuits and the usage of integrated circuits and microprocessors.
C15	CE15/T10: The knowledge and application of the fundamentals of description languages for hardware devices.

Expected results from this subject	Training and Learning Results	
Knowledge of the concepts, components and basic tools of digital design.	B13 B14	C14 C15
Ability to analyse and design combinational systems.	B13	C14 C15
Knowledge of the combinational functional blocks and their aplications.	B14	C14
Knowledge of the basic storage elements, the sequential blocks and their aplications.	B14	C14
Ability to analyse and design synchronous sequential systems.	B13	C14 C15
Knowledge of description and simulation methods based on hardware description languages (HDL).	B13	C14 C15

Contents	
Topic	
Unit 0: Summary	Teaching Staff. Identifying Data. Lecture sessions. Laboratory Sessions. Planning. Assessment. Lecture Scheduling. Laboratory Scheduling. Bibliography.
Unit 1: Introduction to Digital Electronics	Introduction. Number Systems and Digital Codes. Boolean Algebra. Truth tables. Logic Gates. Logic Circuits. Simplyfing logic funcions. Combinational Systems Design with Logic Gates.

Unit 2: Introduction to VHDL	Relevant Language Elements and Concepts for this Course.
Unit 3: Basic Combinational Systems (I)	Functional Blocks. Technologies and Output Types of the Digital Circuits. Decoders.
Unit 4: Basic Combinational Systems (II)	Multiplexers. Encoders. Demultiplexers. Programmable Memories or Look-Up Tables (LUT).
Unit 5: Arithmetic Systems	Comparators. Parity Detection and Generation. Arithmetic Circuits. Application Examples. VHDL Description.
Unit 6: Sequential Logic Systems Principles	Definition and Classification. Latches and flip-flops. Application Examples. VHDL Description.
Unit 7: Synchronous Sequential Systems	Registers. Counters. Shift Registers. Application examples. VHDL description.
Unit 8: Control Synchronous Sequential Logic Design	Control Synchronous Sequential Systems Design. Application Examples. VHDL Description.
Unit 9: Memory Units	Classification. Active and Pasive Random Access Memories (RAM and ROM). Content Access Memories (CAM). Sequential Access Memories (LIFO, FIFO, Circulars).
Practice 1	Introduction to Design using VHDL and the Vivado Design Tool (I).
Practice 2	Introduction to Design using VHDL and the Vivado Design Tool (II).
Practice 3	Combinational System Design and Implemetation (I).
Practice 4	Combinational System Design and Implemetation (II).
Practice 5	Combinational System Design and Implemetation (III).
Practice 6	Combinational System Design and Implemetation (IV).
Practice 7	Arithmetic Circuits.
Practice 8	Arithmetic Systems.
Practice 9	Sequential Circuits.
Practice 10	Sequential Systems (I).
Practice 11	Sequential Systems (II).
Practice 12	Sequential Systems (III).

Planning

	Class hours	Hours outside the classroom	Total hours
Introductory activities	1	0	1
Lecturing	17	20	37
Laboratory practical	24	22	46
Problem solving	13	20	33
Laboratory practice	2	2	4
Problem and/or exercise solving	6	24	30

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies

	Description
Introductory activities	Subject presentation. Presentation of laboratory sessions, instrumentation and software resources to be used.
Lecturing	The lecturer will explain in the classroom the main contents of the subject. The students have to manage the proposed bibliography to carry out a self-study process in a way that leads to acquire the knowledge and the skills related to the subject. The lecturer will answer the students questions in the classroom or in the office. In these sessions the students will develop the skils C14 and C15 ("know").
Laboratory practical	Activities designed to apply the main concepts and definitions of the subject. The students will be asked to acquire the basic skills to manage the laboratory instrumentation, software tools and components in order to construct and test electronic circuits. The students have to develop and demonstrate autonomous learning and collaborative skills. Possible questions can be answered in the laboratory sessions or in the lecturers office. In these sessions the students will develop the skils C15, B13 and B14 ("know how"). Software to be used: VIVADO of Xilinx.
Problem solving	Activities designed to apply the main concepts of the subject to solve problems and exercices. The lecturer will explain a set of problems and the students have to solve diferent take-home sets of problems. The lecturer will answer the students questions in the classroom or at the office. In these sessions the students will develop the skils C14 and B15 ("know how").

Personalized assistance

Methodologies	Description

Lecturing	The lecturer will answer the students questions and also give instructions to guide the studying and learning process. The timetable will be available on the subject website at the beginning of the term. The tutoring sessions will take place, prior appointment by email (sperez@uvigo.gal), in the EEI office #235 or through remote mode in virtual room 1958.
Problem solving	The lecturer will answer the students questions and also give instructions to guide the studying and learning process. The timetable will be available on the subject website at the beginning of the term. The tutoring sessions will take place, prior appointment by email (sperez@uvigo.gal), in the EEI office #235 or through remote mode in virtual room 1958.
Laboratory practical	The teacher will answer the students questions and also give instructions to guide the studying and learning process. The timetable will be available on the subject website at the beginning of the term. The tutoring sessions will take place, prior appointment by email (sperez@uvigo.gal), in the EEI office #235 or through remote mode in virtual room 1958.

Assessment

	Description	Qualification	Training and Learning Results	
Laboratory practical	The lecturer will check the level of compliance of the students with the goals related to the laboratory skills. Final mark of laboratory, FML, will be assessed in a 10 points scale. For the evaluation of the laboratory sessions, the lecturer will assess the group work (the same mark for each member) and the individual answers to personalized questions for each session (individual mark).	30	B13 B14	C15
Problem and/or exercise solving	The lecturer will check the students' skills to solve exercices and troubleshooting. Marks for each test will be assessed in a 10 points scale. Final mark of theory, FMT, will be assessed in a 10 points scale.	70		C14 C15

Other comments on the Evaluation

1. Continuous assessment in ordinary opportunity

Following the own degree's guidelines and the agreements of the academic committee, students who take this subject will be provided with a **continuous assessment** system.

O estudantado que opte por avaliación global deberá notificalo por escrito ao coordinador da materia no prazo dun mes dende o inicio do cuadrimestre.

*Those students who **opt for a global assessment** must send a written notification to the subject coordinator within one month from the beginning of the term.*

The subjetc assessment comprises two parts: theory and practice. The grades obtained in the assessable tasks will be only valid for the ongoing academic year.

1.a. Theory

The intermediate assessment test (PEI) will be held throughout the semester. The date on which it takes place will be approved by the Degree Academic Committee (CAG) and will be available at the beginning of the semester.

The final assessment test (PEF) will be held at the end of the course, on the date established by the CAG.

Each of these tests will consist of a series of short answer questions and/or problem solving and/or exercises and will be scored from 0 to 10 marks.

1.b. Practice

There will be a set of twelve 2-hour laboratory sessions with 2-student groups, whenever possible.

The first four sessions will be guided, aiming at learning the tool management that will be used for the design of digital systems to be implemented into programmable devices. These first four practices are mandatory but will not be scored. In the same way, sessions 5, 7 and 10 are compulsory but will not be scored either.

Nevertheless, sessions 6, 8, 9, 11 and 12 will be graded through continuous assessment.

Each session will be only assessed on the corresponding day and hours to its completion according to the practice schedule and the laboratory group assigned by the centre.

Each session will be scored with a grade (NP) between 0 and 10 marks. The teaching staff will take into account the student previous work to prepare the proposed tasks and the work in the laboratory as well as the student attitude in their posts.

The score for the sessions will be 0 for students who do not attend without any compelling and justified issue.

Laboratory sessions' mark (NP) will be:

NP = (NP6 + NP8 + NP9 + NP11 + NP12) / 5.

In the case of missing more than 2 sessions, the final grade will be:
NP = min{3 ; (NP6 + NP8 + NP9 + NP11 + NP12) / 5}.

1 C. Call's assessment

The continuous assessment mark in ordinary opportunity, which is the one that will appear in the acta, is calculated as follows:
NECOD = 0.3.NP + 0.3 PEI + 0.4 PEF

2. Global assessment in ordinary opportunity

Those who discard the continuous assessment must take two tests: the theory one (EGT), which includes all the subject contents, and the laboratory one (EGP), which includes all the concepts involved in the laboratory sessions. Both tests will be scored between 0 and 10 points.

The global assessment grade in global opportunity, which will be the one that will appear in the acta, is calculated as follows:
NEGOD = 0.5 EGP + 0.5 EGT

3. Continuous assessment in extraordinary opportunity

In this case, the mark obtained in the laboratory sessions (NP) will be kept. The exam (EECOE), which includes all the subject contents, will be scored between 0 and 10 points.

The continuous assessment mark in extraordinary opportunity, which will be the one that will appeared in the acta, is calculated as follows:
NECOE = 0.3 NP + 0.7 EECOE

4. Global assessment in extraordinary opportunity

Those who discard the continuous assessment in the extraordinary opportunity must take two tests: the theory one (EGTE), which includes all the subject contents, and the laboratory one (EGPE), which includes all the concepts involved in the laboratory sessions. Both tests will be scored between 0 and 10 marks.

The global assessment mark in extraordinary opportunity, which will be the one that will appear in the acta, is calculated as follows:
NEGOE = 0.5 EGPE + 0.5 EGTE

5. Assessment of the final degree call

Those who sit this exam must take two tests: the theory one (CFCT), which includes all the subject contents, and the laboratory one (CFCP), which includes all the concepts involved in the laboratory sessions. Both tests will be scored between 0 and 10 marks.

The assessment mark of this call, which will be the one that will appear in the acta, is calculated as follows:
NCFC = 0.5 CFCP + 0.5 CFCT

Sources of information

Basic Bibliography

Wakerly J. F., **Digital Design. Principles and Practices**, 4th, Pearson/Prentice Hall, 2007

E. Mandado, **Sistemas Electrónicos Digitales**, 10ª, Marcombo, 2015

Douglas L. Perry, **VHDL : programming by example**, 4th, McGraw-Hill, 2002

Complementary Bibliography

Thomas L. Floyd, **Digital Fundamentals**, 11th, Pearson, 2014

L.J. Álvarez, E. Mandado, M.D. Valdés, **Dispositivos Lógicos Programables y sus aplicaciones**, 1ª, Thomson-Paraninfo, 2002

S. Pérez, E, Soto, S. Fernández, **Diseño de sistemas digitales con VHDL**, Thomson-Paraninfo, 2002

L.J. Álvarez, **Diseño Digital con Lógica Programable**, 1ª, Tórculo, 2004

J. Bhasker, **A VHDL primer**, 3rd, Prentice Hall, 1999

Recommendations

Subjects that continue the syllabus

Subjects that are recommended to be taken simultaneously

Physics: Fundamentals of electronics/V05G301V01201

Subjects that it is recommended to have taken before

Informatics: Computer Architecture/V05G301V01109