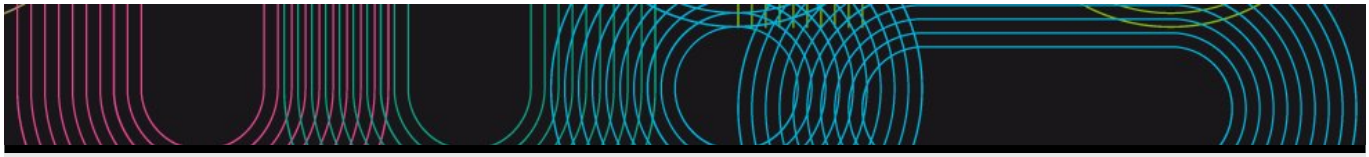

IDENTIFYING DATA				
Electronic Systems for Signal Processing				
Subject	Electronic Systems for Signal Processing			
Code	V05G301V01312			
Study programme	Grado en Ingeniería de Tecnologías de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Optional	3rd	1st
Teaching language	#EnglishFriendly Spanish			
Department				
Coordinator	Valdés Peña, María Dolores			
Lecturers	Valdés Peña, María Dolores			
E-mail	mvaldes@uvigo.es			
Web	http://moovi.uvigo.gal/course			
General description	This subject introduces the basic concepts of digital signal processing systems from the point of view of its hardware implementation. Emphasis is put on FPGAs-based solutions, using professional software design tools and hardware supports. The nature of the course is mainly practical. It promotes the development of collaborative projects whose ultimate goal is the design of electronic signal processing systems. English Friendly subject: International students may request from the teachers: a) materials and bibliographic references in English, b) tutoring sessions in English, c) exams and assessments in English.			

Training and Learning Results	
Code	
B4	CG4: The ability to solve problems with initiative, to make creative decisions and to communicate and transmit knowledge and skills, understanding the ethical and professional responsibility of the Technical Telecommunication Engineer activity.
B6	CG6: The aptitude to manage mandatory specifications, procedures and laws.
B9	CG9: The ability to work in multidisciplinary groups in a Multilanguage environment and to communicate, in writing and orally, knowledge, procedures, results and ideas related with Telecommunications and Electronics.
B13	CG13 The ability to use software tools that support problem solving in engineering.
C39	(CE39/SE1): The ability to construct, exploit and manage the receiving, transporting, representation, processing, storage, manage and presentation multimedia information from the electronic systems point of view.
C45	(CE45/SE7): The ability to design interface, data capturing and storage devices, and terminals for services and telecommunication systems.
D2	CT2 Understanding Engineering within a framework of sustainable development.
D4	CT4 Encourage cooperative work, and skills like communication, organization, planning and acceptance of responsibility in a multilingual and multidisciplinary work environment, which promotes education for equality, peace and respect for fundamental rights.

Expected results from this subject	Training and Learning Results		
Understand the fundamental design principles of the signal processing hardware systems.	B6 B13	C39 C45	
Ability to decide different design strategies depending on the application.	B4	C39 C45	D2
Ability to choice the most suitable hardware architecture for each application.	B4 B6	C39 C45	

Ability to design basic circuits for audio and image processing.	B4 B6 B9 B13	C39 C45	D4
Acquire skills in the use of design, simulation and implementation tools of signal processing systems.	B13	C39 C45	
Acquire skills to verify the proper operation of complex hardware systems.	B6 B13	C39 C45	
Acquire skills to combine different software tools and hardware platforms.	B13	C39 C45	
Ability to document hardware design projects.	B4 B9		D4

Contents	
Topic	
Theory: Theme 1. Introduction	- Basic architecture of electronic signal processing systems: signal conditioning, sampling, conversion, and reconstruction.
Theory: Theme 2. Types of signal processing	-Different hardware and software solutions: DSP and FPGAs. -Processing types: Serial/Parallel, Hardware/Software. -Hardware cost of regular signal processing circuits. Logical resources used. Processing rate.
Theory: Theme 3. Arithmetic in DSP	-Data types. -Data modification: quantification and overflow. -Arithmetic operations and associated circuits. -Associated concepts: critical path, pipeline and latency.
Theory: Theme 4. Signal conditioning and sampling	- Example of a real signal conditioning and sampling system using a FPGA-based development board.
Theory: Theme 5. Design and Implementation of Digital Filters	- Implementation of digital filters in FPGA. - Analysis of full parallel and semi-parallel solutions: hardware costs, operation rates.
Theory: Theme 6. Design of audio processing systems	- Examples of audio processing systems. - Analysis of required hardware resources. - Implementation and performance analysis.
Theory: Theme 7. Design of image processing systems	- Examples of basic image processing systems. - Analysis of hardware resources required. - Implementation and performance analysis.
Labs: Design of basic signal processing systems.	- Design, implementation and verification of basic signal processing systems using VHDL: digital filters, communication applications, image processing, audio processing. - Using the ISE and/or Vivado design tool from Xilinx and MATLAB from MathWorks.

Planning			
	Class hours	Hours outside the classroom	Total hours
Introductory activities	1	0	1
Lecturing	14	14	28
Laboratory practical	14	14	28
Project based learning	9	48	57
Presentation	0	6	6
Problem and/or exercise solving	2	6	8
Laboratory practice	0	14	14
Project	1	3	4
Presentation	1	3	4
*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.			

Methodologies	
	Description
Introductory activities	The teacher will present the theoretical ad practical key topics of the subject, as well as the projects to be developed during the course. B6, C39 and C45 competencies will be worked on. It is an individual activity.

Lecturing	The theoretical content of the course and the introductory activities of both the theoretical and practical contents will be presented. B6, C39 and C45 competencies will be worked on. It is an individual activity.
Laboratory practical	The students will implement basic signal processing systems using FPGAs platforms. B6, B9, C39, C45 and B13 competencies will be worked on. It is a group activity. Software to be used: Matlab, ISE and/or Vivado
Project based learning	Working groups of two or more students will be established. Each group will develop one project along the course. This project will address the design of a signal processing system of medium complexity. Additionally, small groups (Groups Type C) will be available allowing supervising the project developed during the course. Activities to be developed in C groups: Activity 1. Analysis and discussion of the system designed in the project. Activity 2. Demonstration of the operation of the designed system. Analysis and discussion of the results. B6, B9, C39, C45, B13, D2, B4 and D4 competencies will be worked on. It is a group activity. Software to be used: Matlab, ISE and/or Vivado
Presentation	Exhibition by the students to the teacher and to the rest of the students of the results of the developed project. B4, B9 and D4 competencies will be worked on. It is a group activity. Software used: Power Point or any other presentation tool.

Personalized assistance

Methodologies	Description
Lecturing	The teacher will personally attend student□s doubts and queries related to theoretical contents. Students will have the opportunity to attend individual or group tutorials upon request and confirmation via email. The professor's contact data are accessible at https://moovi.uvigo.gal/user/profile.php?id=11303
Laboratory practical	The teacher will personally attend student□s doubts and queries related to laboratory practices. Students will have the opportunity to attend individual or group tutorials upon request and confirmation via email. The professor's contact data are accessible at https://moovi.uvigo.gal/user/profile.php?id=11303
Project based learning	The teacher will personally attend student□s doubts and queries related to the projects. Students will have the opportunity to attend individual or group tutorials upon request and confirmation via email. The professor's contact data are accessible at https://moovi.uvigo.gal/user/profile.php?id=11303

Assessment

	Description	Qualification	Training and Learning Results
Problem and/or exercise solving	There will be a short-answer test on the theoretical issues of the course. More information is provided in the "Other Comments" section below. This test will assess competencies C39 and C45.	20	C39 C45
Laboratory practice	Laboratory practices will be evaluated based on the continuously work carried out during the laboratory hours (Type B hours) and on a final report of the practices. These practices will assess competencies B4, B6, B13, C39, C45 y D4.	35	B4 B6 B13 C39 C45 D4

Project	The students will develop a project focused on the design of a signal processing system of medium complexity. More information is provided in the "Other Comments" section that follows. This project will assess competencies B4, B6, B9, B13, C39, C45, D2 and D4.	40	B4 B6 B9 B13	C39 C45	D2 D4
Presentation	The project will be presented orally. More information is provided in the "Other comments" section. This activity will assess competencies B4, B9 and D4.	5	B4 B9		D4

Other comments on the Evaluation

According to the guidelines for the degree programme, two evaluation systems will be offered to students: continuous assessment (CA) and global assessment (GA).

It is considered that a student opts for CA when he/her takes more than two laboratory practices. In no case can the final grade of a student who opts for CA be "No Submitted". However, the CA may be waived and the GA may be opted for, upon request by email, within a maximum period of one month before the end of the semester.

1.- Continuous assessment

The continuous assessment, both the ordinary and the extraordinary call, consists of a theoretical exam, a set of laboratory practices, a theoretical-practical work (project)and the oral presentation of the project.

The schedule of the assessment activities will be published in a shared calendar and will be available at the beginning of each academic semester.

1.1 Theoretical exam (NExam):

The theoretical exam will include all the theoretical contents of the course and will take place at the end of the term. The weight of this assessment will be 2 points out of 10.

1.2 Laboratory practices (NPrac):

The laboratory practices will be performed in groups of two or more students. The evaluation of the labs will take in to account both, the work in the laboratory as well as a final report. The weight of this assessment is 3.5 point out of 10. The work in the laboratory will be individually evaluated and represent the 60% of the score. The remaining 40% correspond to the final report and will be the same for all the members of a working group.

Laboratory practices are compulsory. To cualify for a practical mark, students must attend at least 80% of the practices.

1.3 Theoretical-practical work (NPro):

The theoretical-practical work will be conducted in type B and C hours, in groups of two or more students. As a result of the work a writing report and the implemented system must be delivered. The weight of this assessment is 4 points out of 10.

To carry out the theoretical-practical work individual and cooperative tasks will be assigned to the students. The weight of the individual work will be the 60% of the maximum score of the project and the weight of the cooperative work will be the 40%. The 40% of the score corresponding the cooperative work will be the same for all the members of a working group.

1.4 Oral presentation of the theoretical-practical work (NPre):

The students must present the results of the theoretical-practical work. The weight of this activity is 0.5 points out of 10. The oral presentation will be at the end of the semester, on the same date as the theoretical exam.

1.5 Final grade (Final_grade):

The final grade for the continuous assessment correspond to:

Final_grade = (0.2*NExam + 0.35*NPrac + 0.4*NPro + 0.05*NPre) if Nexam, NPrac and NPro are greater or equal to 4 and Final_grade is greater or equal to 5;

Final_grade = min[(0.2*NExam + 0.35*NPrac + 0.4*NPro + 0.05*NPre), 4.9] in any other case.

Students who fail any of the assessment activities in the ordinary call will have the possibility to repeat it/them in the extraordinary call. In this case the students would be evaluated only of the part they have not pass (theoretical exam, laboratory practices and/or project). The grade obtained in the extraordinary call will replace the previous one.

2.- Global assessment and End-of-program exam

Students who opt for the global assessment or for the end-of-program exam must pass two assessments, a theoretical one covering all the contents of the subject and a practical one.

2.1 Theoretical exam (NExam_G):

The theoretical examination would include short answer questions, problems, and/or system design exercises.

2.2 Practical exam (NPra_G):

The practical examination will consist in the final test of a previously designed and simulated system. One week before the date established for the exam the student must submit a writing report of the designed system as well as the simulation results. During the practical exam the student will validate the system designed in the hardware.

Both the theoretical and the practical exam will weigh 50% of the final grade.

2.3 Final grade (Final_grade_G):

The final grade of the global assessment and the end-of-program exam will correspond to:

Final_grade_G = (0.5*NExam_G + 0.5*NPrac_G) if Nexam_G and NPrac_G are greater or equal to 4 and Final_grade_G is greater or equal to 5;

Final_grade_G = min[(0.5*NExam_G + 0.5*NPrac_G), 4.9] in any other case.

Students who opt for the global assessment and do not pass the subject in the ordinary call, will have another opportunity in the extraordinary call. In this case, only the part(s) they have failed (theory and/or practice) will be evaluated

3.- Other comments

- The students can use the Spanish, English or Galician to answer the exam an for the reports, works or presentations.
- The grades obtained from the continuous assessment or for the global assessment are only valid for the current academic year.
- The use of books, notes or electronic devices such as phones or computers is not permitted in any classroom test or exam. Mobile phones must be turned off and be out of reach of the student.
- Plagiarism is regarded as serious dishonest behavior. If any form of plagirism is detected in any of the test or exams, the final grade will be FAIL (0), and the incident will be reported to the corresponding academic authorities for prosecution.
- In the event that a student leaves a work group or commits plagiarism, his/her final grade will be FAIL (0), but it will not affect the grade of the rest of the group.

Sources of information

Basic Bibliography

U. Meyer-Baese, **Digital signal processing with Field Programmable Gate Arrays**, 3th ed., Springer-Verlag, 2007

James H. McClellan, Ronald W. Schafer, Mark A. Yoder, **Signal processing first**, 1st ed., Pearson Education International, 2003

XUP, University of Strathclyde and Steepest Ascent, **DSP for FPGA Primer**, 2011

Complementary Bibliography

John G. Proakis, Dimitris G. Manolakis, **Digital signal processing**, 4th ed., Pearson Education International, 2007

John G. Proakis, **Tratamiento digital de señales : principios, algoritmos y aplicaciones**, 4ª ed., Prentice Hall, 2007

Recommendations

Subjects that it is recommended to have taken before

Digital electronics/V05G301V01203