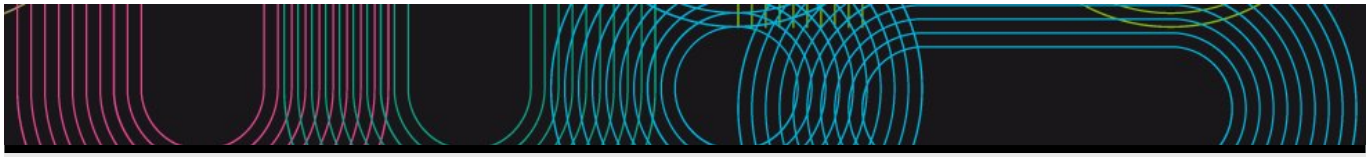

IDENTIFYING DATA				
(*)Sistemas Electrónicos Dixitais Avanzados				
Subject	(*)Sistemas Electrónicos Dixitais Avanzados			
Code	V05M145V01203			
Study programme	(*)Máster Universitario en Enxeñaría de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	5	Mandatory	1st	2nd
Teaching language	Spanish English			
Department				
Coordinator	Moure Rodríguez, María José			
Lecturers	Moure Rodríguez, María José Valdés Peña, María Dolores			
E-mail	mjmoure@uvigo.es			
Web	http://faitic.uvigo.es			
General description	The objective of this course is to provide students with the ability to design complex or high frequency digital systems. Firstly, the electrical characteristics, power consumption, speed and fan-out of digital integrated circuits and the technologies of semiconductor memories are studied. Subsequently, the interface with external peripherals and the methodology for designing synchronous sequential systems are analyzed. Finally, the course focuses on the design of digital communications systems implemented using high density of integration programmable circuits. Meanwhile, throughout all contents, emphasis is placed in the VHDL description of high complexity digital systems.			

Competencies	
Code	
A4	CB4 Students must communicate their conclusions, and the knowledge and reasons stating them-, to specialists and non-specialists in a clear and unambiguous way.
A5	CB5 Students must have learning skills to allow themselves to continue studying in largely self-directed or autonomous way
A9	CG4 The capacity for mathematical modeling, calculation and simulation in technological centers and engineering companies, particularly in research, development and innovation tasks in all areas related to Telecommunication Engineering and associated multidisciplinary fields.
A13	CG8 The ability to apply acquired knowledge and to solve problems in new or unfamiliar environments within broader and multidiscipline contexts, being able to integrate knowledge.
A28	CE10 The ability to design and manufacture integrated circuits.
A29	CE11 The knowledge of hardware description languages for high complexity circuits.
A30	CE12 The ability to use programmable logic devices, as well as to design advanced electronic systems, both analog and digital. The ability to design communications components such as routers, switches, hubs, transmitters and receivers in different bands.
A32	CE14 The ability to develop electronic instrumentation, as well as transducers, actuators and sensors.

Learning aims		
Expected results from this subject	Typology	Training and Learning Results
The knowledge of the different technologies of integrated circuits manufacture.	know	A28
The ability to analyze and design advanced digital circuits.	Know How	A30
The knowledge of different input/output technologies of digital circuits.	know	A32
The ability to design input/output interface circuits.	Know How	A28
The knowledge of the methodologies for the design of complex digital circuits.	know	A30 A32

The ability to design communication components using programmable logic devices.	Know How	A4 A5 A13 A30
The ability to design complex digital electronic systems using hardware description languages.	Know How	A9 A29

Contents	
Topic	
Topic 1: Technologies of digital integrated circuits	CMOS technology: logic gates, electrical characteristics, fan-out, delay, power consumption, logic families. Competency A28.
Topic 2: Semiconductor memories	SRAM and DRAM memories, EEPROM. FLASH and PCM memories. Memory expansion. Design of memory interfaces. VHDL description. Competencies A28, A29 and A30.
Topic 3: Input/output interfaces	Interface with peripherals and A/D and D/A converters. Interfaces with communication buses. VHDL description. Competencies A29, A30 and A32.
Topic 4: Design of sequential synchronous systems	Finite state machines. Synchronization methods. Generation and propagation of clocks signals. Competencies A29 and A30.
Topic 5: Hardware implementation of digital communication systems	Sampling, quantification, coding, arithmetic circuits, frequency synthesis. VHDL description. Competencias A29 and A30.
Topic 6: Design of complex digital systems using FPGAs	Advanced architectures of FPGAs. IP blocks. Multirate systems. Parallel processing. VHDL description. Competencies A29, A30 and A32.
Laboratory Practices	- Design of a storing and data transference system. - Design of a complex interface with standard peripherals. Competencies A4, A9, A29, A30 and A32.

Planning			
	Class hours	Hours outside the classroom	Total hours
Master Session	17	25	42
Laboratory practises	10	5	15
Projects	9	30	39
Short answer tests	3	20	23
Practical tests, real task execution and / or simulated.	0	5	5
Jobs and projects	1	0	1
*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.			

Methodologies	
	Description
Master Session	The professor explains the theoretical contents of the course, encouraging critical discussion and the student involvement. Reading assignments for each session will be previously available via FaiTIC, and students are expected to come to the theoretical class having completed the assigned reading. In these sessions students work the competencies A4, A5, A28, A29, A30 y A32.
Laboratory practises	During laboratory sessions students apply the design methods described in the master sessions. All the sessions are guided and supervised by the professor. The in-person sessions are developed in a laboratory with skilled equipment. In the laboratory sessions students acquire the competencies A4, A9, A29, A30 y A32.
Projects	This activity focuses on applying the techniques described in the lecture classes and the skills developed at laboratory to a project implementation. The in-person sessions are developed in a laboratory with skilled equipment. Students should obtain well founded solutions, choosing appropriate methods and devices. These projects are planned and tutored in small size groups. By means of this project students work the competencies A4, A5, A9, A 13, A29, A30 y A32.

Personalized attention	
Methodologies	**Description**

Master Session	Students have the opportunity to solve doubts in personalized attention sessions. The appointment with the corresponding professor should be required and agreed by e-mail, preferably in the timetable and place officially assigned. Besides, the group of students developing a project will attend periodic follow-up meetings.
Laboratory practises	Students have the opportunity to solve doubts in personalized attention sessions. The appointment with the corresponding professor should be required and agreed by e-mail, preferably in the timetable and place officially assigned. Besides, the group of students developing a project will attend periodic follow-up meetings.

Tests	**Description**
Jobs and projects	Students have the opportunity to solve doubts in personalized attention sessions. The appointment with the corresponding professor should be required and agreed by e-mail, preferably in the timetable and place officially assigned. Besides, the group of students developing a project will attend periodic follow-up meetings.

Assessment

	Description	Qualification
Short answer tests	There are 2 objective tests, the estimated date of the first will be after the completion of the 50% of the theoretical classes and the second after the completion of all of them. Both tests cover all of the contents taught in the theoretical classes. The first test will deserve the 20% and the second the 30% of the final qualification. These tests will assess the competencies A28, A29, A30 y A32.	50
Practical tests, real task execution and / or simulated.	The assistance to the laboratory practices is mandatory and the student should complete at least 4 of the 5 sessions. The implementation of the circuits described in the practice guidelines and the reports submitted at the end on each session will deserve the 20% of the final qualification. These practical developments will assess the competencies A5, A9, A29, A30 y A32.	20
Jobs and projects	The students should present a tutored project which deserves the 30% of the final qualification. The progress of this job will be supervised from continuous assessment but the final work should be oral presented by the authors. This project will assess the competencies A4, A5, A9, A13, A29, A30 y A32.	30

Other comments on the Evaluation

1. Continuous assessment

The course can be passed with full marks from continuous assessment, with no need to sit the final exam. Students who assist to more than 2 laboratory sessions or to the first test are graded using continuous assessment.

The weighting and content of each continuous assessment part are as follows:

1.1 Test (NExam):

- It covers all of the contents taught in the theoretical classes.
- The estimated date of the first test (NExam1) will be the middle week of the course.
- The date of the second test (NExam2) will be the same of the final exam.
- The mark NExam is obtained as follows:

  NExam = NExam1*0.4 + NExam2*0.6

- The student pass this part if he/she gets a mark greater than or equal to 4 over 10.

1.2 Laboratory practices (NPrac):

- The student should complete 4 of the 5 sessions in order to pass this part.
- The student should correctly implement the circuits described in the guidelines of the practice and submit a report corresponding to each laboratory session. The qualification of each practice depends on these achievements.
- It can be developed individually or by groups of 2 students.

1.3 Project (NPro):

- It can be developed individually or by groups of 2 students.
- It should be oral presented by the authors.

- The student will pass this part if he/she gets a mark greater than or equal to 4 over 10.

1.4 Final qualification of continuous assessment (Final_ca)

The final qualification (Final_ca) of continuous assessment is obtained as follows:

Final_ca: = (NExam*0.5 + NPrac*0.2 + NPro*0.3) if NExam and Npro are greater than or equal to 4;

Final_ca = min [(NExam*0.5 + NPrac*0.2 + NPro*0.3), 4.5] in other case;

The student who fails one or more of the parts of continuous assessment has another opportunity to pass the following parts in the final exam:

- He/she can repeat the first test (NExam1) and this mark replaces the previous one.
- He/shet can complete and present his/her project before the date of the final exam and this mark replaces the previous one.

2. Final exam and qualification

There is a final exam at the end of the bimester and in July.

- In the final exam, all content is evaluated. It usually consists of several questions and problems and lasts 2 hours. The pass mark for this exam is 4 out of 10 and deserves 50% of the final qualification (NExam).
- The students must present the results and reports of the same practices developed in continuous assessment. This practices represent 20% of the final qualification (NPrac).
- In order to pass the subject the students should present a project with the same objectives and complexity of the project developed in continuous assessment. This project deserves 30% of the final qualification (NPro) and it is necessary to obtain a mark greater o equal to 4 out of 10 in order to pass the course.

Final_ex = (NExam*0.5 + NPrac*0.2 + NPro*0.3) if NExam and Npro are greater than or equal to 4;

Final_ex = min [(NExam*0.5 + NPrac*0.2 + NPro*0.3), 4.5] in other case;

3. Other comments

- The grades obtained from the continuous assessment and final exams are only valid for the current academic year.
- The use of books, notes or electronic devices such as phones or computers is not permitted in any test or exam. Mobile phones must be turned off and be out of reach of the student.

Sources of information

Neil Weste, David Harris, **CMOS VLSI Design. A circuits and systems perspective**, 4ª,

Ashok K. Sharma, **Semiconductor memories : technology, testing, and reliability**,

Charles H. Roth, Jr., Lizy Kurian John, **Digital systems design using VHDL**, 2ª,

Santosh K. Kurinec, Krzysztof Iniewski, **Nanoscale Semiconductor Memories: Technology and Applications (Devices, Circuits, and Systems)**,

William Kleitz, **Digital Electronics: A Practical Approach with VHDL**, 9ª,

David J. Comer, **Digital logic and state machine design**, 3ª,

John F. Wakerly, **Digital Design. Principles and Practices**, 4ª,

In addition to the bibliography above, the student have access to the following support material:

- Slides of the course which cover the contents of theoretical sessions.
- Documentation for laboratory which includes the guidelines of the practices, the manual of the CAD tools and the data sheets of the devices.

This material is available via the FaiTIC platform (http://faitic.uvigo.es)

Recommendations