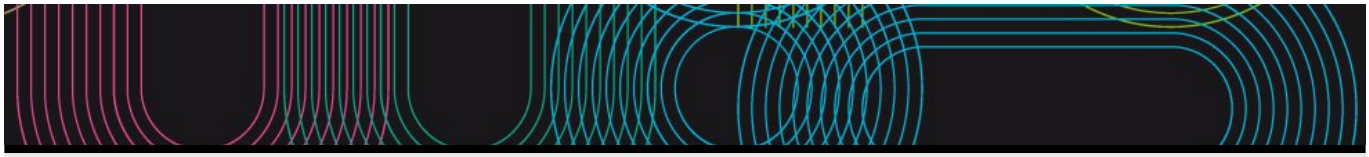

IDENTIFYING DATA				
Microelectronics Design				
Subject	Microelectronics Design			
Code	V05G306V01317			
Study programme	Grado en Ingeniería de Tecnologías de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Optional	3rd	2nd
Teaching language	#EnglishFriendly Spanish			
Department				
Coordinator	Cao Paz, Ana María			
Lecturers	Cao Paz, Ana María Rodríguez Pardo, María Loreto			
E-mail	amcaopaz@uvigo.es			
Web	http://moovi.uvigo.gal			
General description	The main purposes of this course are for the students: 1) To get acquainted with integrated circuits (ICs) and micro-electro-mechanical systems (MEMs) fabrication technologies. 2) To get acquainted with CMOS fabrication processes for ICs and MEMs. 3) To analyze the physical structure of passive components and active devices in CMOS technology. 4) To get acquainted with the basic aspects of MEMs design. 5) To work with CAD tools for the design.of CMOS ICs English Friendly subject: International students may request from the teachers: a) materials and bibliographic references in English, b) tutoring sessions in English, c) exams and assessments in English.			

Training and Learning Results	
Code	
B6	CG6: The aptitude to manage mandatory specifications, procedures and laws.
B9	CG9: The ability to work in multidisciplinary groups in a Multilanguage environment and to communicate, in writing and orally, knowledge, procedures, results and ideas related with Telecommunications and Electronics.
B13	CG13 The ability to use software tools that support problem solving in engineering.
C42	(CE42/SE4): The ability to apply electronics as support technology in other fields and activities and not only in information and communication technologies.
C43	(CE43/SE5): The ability to design analogical and digital electronics circuits of analogical to digital conversion and vice versa, of radiofrequency, of feeding and electrical energy conversion for computing and telecommunication engineering.
D4	CT4 Encourage cooperative work, and skills like communication, organization, planning and acceptance of responsibility in a multilingual and multidisciplinary work environment, which promotes education for equality, peace and respect for fundamental rights.

Expected results from this subject	Training and Learning Results		
To know and understand fabrication process of integrated circuits (ICs) and micro-electro-mechanical systems (MEMs) in CMOS technology, as well as design methodologies and steps for the specification of an IC.	B6	C42 C43	
To understand and be able to analyze the physical structure of resistors, capacitors, and transistors for inclusion in CMOS technology ICs.	B6 B9	C43	D4
To be capable of working with CAD tools for the design of CMOS ICs.	B6 B9 B13		D4

To know and understand the basic aspects of analog ICs design and their basic structures in CMOS technology.	C42

Contents	
Topic	
Chapter 1: Introduction (1h)	Course introduction. Purposes and planning of the course. Basic concepts in the design of integrated circuits (ICs) and micro-electro-mechanical systems (MEMs).
Chapter 2: Fabrication steps for ICs and MEMs (2h)	Introduction to ICs and MEMs fabrication. Planar technology. Micromachining and micromolding technologies. CMOS IC fabrication steps. Structure of MOS transistors. Fabrication example: CMOS inverter. Layout. MEMs fabrication steps: bulk micromachining, surface micromachining, and LIGA.
Chapter 3. ICs and MEMs fabrication processes (3h)	Silicon wafers. Epitaxial layers. Dielectric layers. Oxidation. Deposition. Semiconductor layers. Dopant diffusion. Ion implantation. Photolithography. Etching. Metalization.
Chapter 4. Modeling of MOS transistors (3h).	MOS transistors: analytical model. Higher-order effects. Fundamentals of Spice modeling and simulatin. Spice models of MOS transistors.
Chapter 5. Physical structure of basic elements (2h)	Specification of the physical structure of a MOS transistor. Specification of the physical structure of a resistor. Specification of the physical structure of a capacitor. Types of physical specifications. Influence of physical design in the behavior of a device. Design rules. Design methodologies and tools.
Chapter 6. Resistor layout strategies (1h)	Lateral diffusion. Effective geometric dimensions. Influence of the terminals. Long resistors. Unit resistors. Stacked resistors. Neighborhood effects. Dummies. Interdigited and common centroid structures.
Chapter 7. Capacitor layout strategies (1h)	Oxide thickness gradient, lateral diffusion, and neighborhood effects. Area and perimeter unit capacitances.
Chapter 8. Transistor layout strategies (2h)	Transistor with high aspect ratio. Stacked transistors. Interdigited structures.
Chapter 9. Physical design case studies (3h)	Basic current mirror. Self-biased differential amplifier.
Lab assignment 1. Introduction to IC design tools (2h)	Introduction to physical design tools. Basic layout elements and individual nMOS and pMOS transistors. Design Rule Check (DRC). Predesigned elements and transistors.
Lab assignment 2. CMOS inverter (4h)	Schematic design of a CMOS inverter. Corrections for symmetrical response. Simulation with capacitive loads. Layout design and DRC. Layout Versus Schematic (LVS). Post-layout simulation (without and with capacitive load). Comparison with schematic simulation.
Lab assignment 3. MOS transsitor layout strategies (2h)	Layout of pMOS and nMOS transistors. Snake, stacked, and interdigited structures. Dummy structures.
Lab assignment 4. Physical design of analog functional blocks: current mirror and differential pair (3h)	Layouts of a basic curent mirror and a self-biased pMOS differential amplifier.
Lab assignment 5. Passive components layout strategies (2h)	Layouts of resistors and capacitors. Linear, snake, stacked and interdigited structures. Dummy structures.

Planning	Class hours	Hours outside the classroom	Total hours
Lecturing	18	45	63
Practices through ICT	13	19.5	32.5
Project based learning	6	27	33
Presentation	1	2.5	3.5
Problem and/or exercise solving	1	3.5	4.5
Problem and/or exercise solving	2	7	9
Laboratory practice	1	3.5	4.5
*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.			

Methodologies	Description
Lecturing	The professor will present the relevant concepts of the course. Before each lecture, students must carry out a preparatory analysis of the topics to be addressed, aiming at their active participation. Practical examples and case studies will be developed and analyzed. Attendance will be recorded. Competencies C42 and C43 will be addressed in these sessions

Practices through ICT	Students will work using IC CAD tools. All relevant steps in the physical design of an IC will be practically studied. Attendance will be recorded, and performance of each group in each lab assignment will be evaluated. Software to be used: Electric and LTSpice. Competencies C43 and B13 will be addressed in these sessions
Project based learning	Students will work in small teams (C-type groups) in the physical design and characterization of a circuit consisting of active devices and passive components, under the close guidance of professors. Attendance will be recorded. The activities to be developed by each team are: - Analysis of possible solutions and design alternatives. - Critical analysis of the design process developed. - Demonstration of the circuits designed in the project. - Preparation of a report where results are presented, analyzed, and discussed. Competencies C43, B6, B9, B13, and D4 will be addressed in these sessions.
Presentation	Each group of students will publicly present their project to professors and the other students in the group. Anyone in the audience will be allowed to ask questions about the project. Competencies C43, B6, B9, and D4 will be addressed in these sessions.

Personalized assistance

Methodologies	Description
Lecturing	Professors will personally assist students with doubts and questions they may have about either theoretical contents. Office hours will be scheduled for both individual and group sessions. The information to request the personalized assitance can be consulted in the MooVi profile of the teaching team: María Loreto Rodríguez Pardo: https://moovi.uvigo.gal/user/view.php?id=11332 Ana María Cao Paz: https:// moovi.uvigo.gal/user/view.php?id=11331
Practices through ICT	Professors will personally assist students with doubts and questions they may have about lab assignments. Office hours will be scheduled for both individual and group sessions. The information to request the personalized assitance can be consulted in the MooVi profile of the teaching team: María Loreto Rodríguez Pardo: https://moovi.uvigo.gal/user/view.php?id=11332 Ana María Cao Paz: https:// moovi.uvigo.gal/user/view.php?id=11331
Project based learning	Professors will personally assist students with doubts and questions they may have about the development of the projects. Office hours will be scheduled for both individual and group sessions. The information to request the personalized assitance can be consulted in the MooVi profile of the teaching team: María Loreto Rodríguez Pardo: https://moovi.uvigo.gal/user/view.php?id=11332 Ana María Cao Paz: https:// moovi.uvigo.gal/user/view.php?id=11331
Presentation	Professors will personally assist students with doubts and questions they may have about the preparation of the public presentations. Office hours will be scheduled for both individual and group sessions. The information to request the personalized assitance can be consulted in the MooVi profile of the teaching team: María Loreto Rodríguez Pardo: https://moovi.uvigo.gal/user/view.php?id=11332 Ana María Cao Paz: https:// moovi.uvigo.gal/user/view.php?id=11331

Assessment

	Description	Qualification	Training and Learning Results
Project based learning	Each group of students will deliver the design carried out in the project in the format of the integrated circuit design tool. To pass the course, the design must meet technological standards and it shall comply the required specifications. In addition, each group must submit a detailed project report, with explicit information about the contribution of each of them to the whole, as well as the methodology followed for the distribution and coordination of tasks. Based on this division of tasks, it can be assigned an individual mark to each of the group members. The evaluation of the projects will be based on a list of items provided previously. Reports must be submitted on the date indicated in the planning of the course and it will be at least two days prior to the public presentation. To pass the course, students must achieve at least a mark of 5 or higher in a scale of 0-10 in the project (design and reporting). Competencies C43, B6, B9, B13, and D4 will be assessed in these projects.	25	B6 C43 D4 B9 B13

Presentation	Each student must provide an individual 5-minute public presentation of the part of the project he/she carried out (including planning / coordination tasks, if applicable). Presentations will be scheduled in the last (1-hour) classroom session of the corresponding group. At the end of each presentation, the student must give suitable replies to questions from the audience, which will consist of professors and the other students in the group, who must attend the whole session. Evaluation will be based on the content, formal issues, and deliverance of the presentation, as well as on the way the student replies to que questions from the audience. Students asking relevant questions will get additional score for them. The mark obtained in the public presentation consists of two parts, a common part for tasks carried out jointly and an individual part of the exposition of each student of his or her work as well as the appropriate interventions at the end of the exposure of other groups. To pass the course, the student must achieve in his/her presentation (plus additional score if applicable) a mark of 5 or higher in a 0-10 scale. Competencies C43, B6, B9, and D4 will be assessed in these presentations.	5	B6 B9	C43 D4
Problem and/or exercise solving	As part of the continuous assessment, two written individual tests are conducted. The first evaluation 1-hour written test will be held during one of the classroom sessions, covering course contents lectured so far. The test will consist of short answer questions, accounting for 20% of the global mark. The second written test will be held at the end of classroom sessions, covering the remaining classroom contents and accounting for 5% of the global mark. This test will be held in conjunction with the test of design problems or exercises more fully described below. The test will last for about an hour, including written test and design problems (or exercises) test. To pass the course, students must achieve in each of the tests a mark or 4 or higher in a 0-10 scale. Competencies C42 and C43 will be assessed in these tests	25		C42 C43
Problem and/or exercise solving	An exam of troubleshooting and / or exercises will be carried out as part of the continuous assessment, accounting for 15% of the global mark. This exam will be held in conjuction with the second written test described in the previous section and it will last for about an hour as a whole. To pass the course, students must achieve in this exam a mark or 4 or higher in a 0-10 scale. Competencies C42 and C43 will be assessed in this test.	15		C42 C43
Laboratory practice	All students, in continuous evaluation or not, must submit the files of the Lab practices. Deadline for submissions will be communicated sufficiently in advance. These submissions account for 10% of the global mark. All students, in continuous evaluation or not, must submit a complete report based in Lab Assignments 1 and 2 with the achieved results and conclusions according to the indications of the teaching staff. The report is due the indicated date in the planning. The corresponding report account for 10% of the global mark. A continuous evaluation 1-hour lab exam using an IC CAD tool will be held in the last scheduled lab session. Another similar exam will be held in the date of the final exam. It is compulsory for students not in continuous evaluation. Lab tests account for 10% of the global mark. To pass the course, students must achieve a mark or 4 or higher in a 0-10 scale in each part: lab files submissions, Lab Report and the lab test. Competencies C43 and B13 will be assessed in this part.	30	B13	C43

Other comments on the Evaluation

Continous assesment:

The planning of the different tests of intermediate evaluation will be approved by the "Comisión Académica de Grado" (CAG) and it will be available at the beginning of the semester.

In order to pass the course, students must achieve a global mark of 5 or higher in a 0-10 scale. The global mark will be obtained as the weighted summation of the scores obtained in the different parts of the course. A minimum score is required in each of these parts. For students not achieving the minimum score in any of the parts, the global mark will be the lower value between 4.5 and the weighted summation of scores.

Global assessment:

Students not in continuous evaluation will be evaluated as follows:

- Final written and lab tests will account for the same percentage of the global mark as in the case of students in continuous assessment.
- They must develop a project and deliver the corresponding report and public presentation (in the same sessions and with

the same criteria as students in continuous assessment). Reports are due two days before public presentation.
- They must complete all the lab practice files submissions and deliver the Lab written report with the achieved results and conclusions.
Minimum scores in the different parts for students in global assessment are the same as for students in continuous assessment.
The deadline to renounce to continuos assessment will be one month before the end date of the semester, according to the calendar of the center. The procedure will be by sending an email to the teaching staff requesting the renounce of continuous assessment.

Extraordinary call and End-of-program call.

Requirements to pass the course in these calls will be the same as in the continuos assessment, in terms of the minimum scores. Students must complete the two written tests and the lab test. The practice files, the lab report and the memory of the project must be submitted 7 days before the date of the exam.

Sources of information

Basic Bibliography

José Antonio Rubio Solà, **Diseño de circuitos y sistemas integrados**,
Stephen A. Campbell, **Fabrication Engineering at the Micro-and Nanoscale**, 4ª,
J. Franca, Y. Tsividis (eds.), **Design of analog VLSI circuits for telecommunications and signal processing**,

Complementary Bibliography

Recommendations

Subjects that it is recommended to have taken before

Digital electronics/V05G301V01203
Physics: Fundamentals of electronics/V05G301V01201
Electronic technology/V05G301V01206

Other comments

All conclusions achieved both in the written tests and in the projects must be adequately justified. Non-trivial concepts cannot be assumed but they have to be explained. The methodologies used by the student will be taken into account in the computation of his/her marks. No auxiliary resources, including but not limited to documentation, can be used in the written tests.

In case of detection of plagiarism in any of the evaluation tests or assignment submissions, the final grade will be SUSPENSE (0) and the fact will be reported to the corresponding academic authorities for prosecution.