



## IDENTIFYING DATA

### Programmable Electronic Circuits

Subject	Programmable Electronic Circuits			
Code	V05G306V01302			
Study programme	Grado en Ingeniería de Tecnologías de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Mandatory	3rd	1st
Teaching language	English			
Department				
Coordinator	Álvarez Ruiz de Ojeda, Luís Jacobo			
Lecturers	Álvarez Ruiz de Ojeda, Luís Jacobo			
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Web	<a href="http://moovi.uvigo.gal">http://moovi.uvigo.gal</a>			
General description	The documentation of the subject may be in English. The objectives of this course are that students learn the general aspects of the architecture of microprocessors, microcontrollers and configurable devices, as well as the adequate design methods and tools, while they acquire the necessary skills to design systems based on these devices.			

## Training and Learning Results

Code	
B3	CG3: The knowledge of basic subjects and technologies that enables the student to learn new methods and technologies, as well as to give him great versatility to confront and adapt to new situations
B4	CG4: The ability to solve problems with initiative, to make creative decisions and to communicate and transmit knowledge and skills, understanding the ethical and professional responsibility of the Technical Telecommunication Engineer activity.
B13	CG13 The ability to use software tools that support problem solving in engineering.
C7	CE7/T2: The ability to use communication and software applications (ofomatics, databases, advanced calculus, project management, visualization, etc.) to support the development and operation of Electronics and Telecommunication networks, services and applications.
C8	CE8/T3: The ability to use software tools for bibliographical resources search or information related with electronics and telecommunications.
C14	CE14/T9: The ability to analyze and design combinatory and sequential, synchronous and asynchronous circuits and the usage of integrated circuits and microprocessors.
C15	CE15/T10: The knowledge and application of the fundamentals of description languages for hardware devices.
D2	CT2 Understanding Engineering within a framework of sustainable development.
D3	CT3 Awareness of the need for long-life training and continuous quality improvement, showing a flexible, open and ethical attitude toward different opinions and situations, particularly on non-discrimination based on sex, race or religion, as well as respect for fundamental rights, accessibility, etc.

## Expected results from this subject

Expected results from this subject		Training and Learning Results
To understand the basic architecture of microprocessors, microcontrollers and configurable devices (FPGAs).	B3	C14 C15
To know the methods and techniques of design of integrated hardware/software systems (System on Chip □ SoC).	B3	C14 C15
To know the hardware and software tools for the design of systems based in programmable devices.	B13	C14 C15
To acquire the skills to use the design tools for the design of digital systems.		C14 C15

Ability to design simple integrated systems (System on Chip □ SoC) applied to the telecommunications fields.

B3 C7 D2  
B4 C8 D3  
B13 C14  
C15

## Contents

Topic	
LESSON 1 THEORY. ANALYSIS OF DIFFERENT TYPES OF DIGITAL CIRCUITS.	Types of digital circuits. Main characteristics. System on Chip (SOC). Types. Characteristics.
LESSON 2 THEORY. FPGAs. APPLICATIONS. ARCHITECTURE OF THE FAMILY USED.	General architecture of FPGAs. Characteristics. Analysis of the family of FPGAs used in the subject.
LESSON 3 THEORY. CORRECT DESIGN METHODS. SYNCHRONOUS DESIGN.	Digital systems design techniques. Recommendations. Design rules for synchronous sequential systems
LESSON 4 THEORY. DESIGN METHODS OF COMPLEX SYNCHRONOUS DIGITAL SYSTEMS.	Study of a systematic design method for this type of systems.
LESSON 5 THEORY. INTERNAL ARCHITECTURE OF THE MICROPROCESSOR USED IN THE SUBJECT.	Analysis of the internal architecture. Instruction set.
LESSON 6 THEORY. SOFTWARE DEVELOPMENT FOR THE MICROPROCESSOR USED IN THE SUBJECT.	Program syntax. Compilation directives.
LESSON 7 THEORY. EXTERNAL ARCHITECTURE OF THE MICROPROCESSOR USED IN THE SUBJECT.	External architecture of the microprocessor. Signals used for I/O. Connection of I/O peripherals. Interrupts.
LESSON 8 THEORY. DESIGN OF EMBEDDED SYSTEMS. HARDWARE / SOFTWARE CODESIGN.	Hardware/software codesign flow. Partitioning.
LESSON 1 LABORATORY. DESIGN A BASIC DIGITAL SYSTEM IN THE CORRECT FORM.	Design of a digital system using VHDL for its implementation in an FPGA, applying the correct design recommendations.
LESSON 2 LABORATORY. DESIGN OF A COMPLEX SYNCHRONOUS DIGITAL SYSTEM.	Design of a complex digital system using VHDL for its implementation in an FPGA, using the systematic design method analyzed in theory.
LESSON 3 LABORATORY. DESIGN OF A SOC TYPE BASIC EMBEDDED SYSTEM BASED ON AN FPGA (PSOC).	Design of the circuits and development of the necessary programs to implement a basic embedded system in an FPGA, using the microprocessor analyzed in theory.
LESSON 4 LABORATORY. DESIGN OF A MEDIUM COMPLEXITY EMBEDDED SYSTEM.	Design of the circuits and development of the necessary programs to implement an embedded system of medium complexity, combining the basic system previously developed with additional circuits and programs that the student must develop.

## Planning

	Class hours	Hours outside the classroom	Total hours
Introductory activities	2	2	4
Lecturing	12	16	28
Problem solving	12	19	31
Mentored work	6	10	16
Mentored work	6	10	16
Mentored work	6	10	16
Mentored work	8	14	22
Essay questions exam	4	13	17

\*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

## Methodologies

	Description
Introductory activities	Introduction to key topics both theoretical and practical.
	Through this methodology the competence B3 is developed.
Lecturing	Conventional lectures.
	Through this methodology the competence B3 is developed.
Problem solving	In these sessions, exercises will be solved by both the teacher and the students.
	Through this methodology the competences B3, B4, C8, C14 and C15 are developed.
Mentored work	Practical work on the design of a digital system applying the correct design recommendations.
	With this methodology develop the competences B3, B4, B13, C7, C8, C14, C15, D2 and D3.

Mentored work	Practical work on the design of a complex digital system using the systematic design method analyzed in theory.  With this methodology develop the competences B3, B4, B13, C7, C8, C14, C15, D2 and D3.
Mentored work	Practical work on the design of circuits and programs necessary to implement a basic embedded system using the microprocessor analyzed in theory.  With this methodology develop the competences B3, B4, B13, C7, C8, C14, C15, D2 and D3.
Mentored work	Practical work on the design of circuits and programs necessary to implement an embedded system of medium complexity using the microprocessor analyzed in theory.  With this methodology develop the competences B3, B4, B13, C7, C8, C14, C15, D2 and D3.

### Personalized assistance

Methodologies	Description
Introductory activities	In the classes the doubts of the students will be answered. They will also be able to consult with the teachers in the place and at the time published at <a href="https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda">https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda</a> y <a href="https://moovi.uvigo.gal/user/profile.php?id=11302">https://moovi.uvigo.gal/user/profile.php?id=11302</a> .
Lecturing	In the classes the doubts of the students will be answered. They will also be able to consult with the teachers in the place and at the time published at <a href="https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda">https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda</a> y <a href="https://moovi.uvigo.gal/user/profile.php?id=11302">https://moovi.uvigo.gal/user/profile.php?id=11302</a> .
Problem solving	In the classes the doubts of the students will be answered. They will also be able to consult with the teachers in the place and at the time published at <a href="https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda">https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda</a> y <a href="https://moovi.uvigo.gal/user/profile.php?id=11302">https://moovi.uvigo.gal/user/profile.php?id=11302</a> .
Mentored work	In the classes the doubts of the students will be answered. They will also be able to consult with the teachers in the place and at the time published at <a href="https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda">https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda</a> y <a href="https://moovi.uvigo.gal/user/profile.php?id=11302">https://moovi.uvigo.gal/user/profile.php?id=11302</a> .
Mentored work	In the classes the doubts of the students will be answered. They will also be able to consult with the teachers in the place and at the time published at <a href="https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda">https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda</a> y <a href="https://moovi.uvigo.gal/user/profile.php?id=11302">https://moovi.uvigo.gal/user/profile.php?id=11302</a> .
Mentored work	In the classes the doubts of the students will be answered. They will also be able to consult with the teachers in the place and at the time published at <a href="https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda">https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda</a> y <a href="https://moovi.uvigo.gal/user/profile.php?id=11302">https://moovi.uvigo.gal/user/profile.php?id=11302</a> .
Mentored work	In the classes the doubts of the students will be answered. They will also be able to consult with the teachers in the place and at the time published at <a href="https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda">https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda</a> y <a href="https://moovi.uvigo.gal/user/profile.php?id=11302">https://moovi.uvigo.gal/user/profile.php?id=11302</a> .

### Assessment

Description	Qualification	Training and Learning Results
Mentored work Practical work on the design of a digital system applying the correct design recommendations.	10	B3 C7 D2 B4 C8 D3 B13 C14 C15
Mentored work Practical work on the design of a complex digital system using the systematic design method analyzed in theory.	15	B3 C7 D2 B4 C8 D3 B13 C14 C15
Mentored work Practical work on the design of circuits and programs necessary to implement a basic embedded system using the microprocessor analyzed in theory.	15	B3 C7 D2 B4 C8 D3 B13 C14 C15
Mentored work Practical work on the design of circuits and programs necessary to implement a basic embedded system using the microprocessor analyzed in theory.	20	B3 C7 D2 B4 C8 D3 B13 C14 C15

Essay questions exam	This exam will include two types of questions: 1) Multiple choice questions about the theoretical topics of the subject. 2) Design problems about circuits and programs, explaining the work done.	40	B3 B4	C14 C15
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### Other comments on the Evaluation

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The final mark will be expressed in numerical form ranging from 0 to 10.

The students will be offered two assessment systems: continuous assessment and global assessment.

It is considered that all the students have chosen continuous assessment by default.

Choosing of global assessment must be communicated in writing form to the coordinator within one month of the start of the semester.

All the tasks must be delivered in the date specified by the professor, otherwise they will not be assessed.

In case of detection of plagiarism in any of the tasks (theoretical exam, laboratory practices or autonomous projects) the final qualification will be fail (0) and the fact will be communicated to the Head of the faculty for further actions.

The subject is composed of a theoretical part and a laboratory part, with a respective weighting of 40% and 60% of the total mark of the subject.

The theoretical part consists of a final examination. This final examination will be the same for all the students, regardless of the type of assessment they have opted for.

The exam will be on the date of the final exam of the semester, which the faculty will determine.

#### **CONTINUOUS ASSESSMENT (ordinary exam)**

Laboratory class attendance is compulsory if the student is following continuous assessment.

The students who are following continuous assessment can only miss 1 laboratory session without justification, as a maximum.

If the number of students in any laboratory group is sufficiently small, the students will carry out the practices and projects individually. Otherwise, students will perform these tasks in groups of 2. In the latter case, the two students will receive the same mark.

Theoretical class attendance is considered crucial to achieve success in continuous assessment, as the experience shows that it has a strong influence on the rate of success in the continuous assessment.

All the tasks have to be delivered on the date specified by the professor, otherwise they will not be assessed. It is also compulsory to sit the theoretical exam in the continuous assessment.

None of the tasks can be done on a different date than the one set up by the professor.

If any of the previous conditions is not met, the student that was in continuous assessment will lose the right to it and will automatically fail.

The total mark will be the weighted sum of the marks obtained in the different tasks of the subject.

To pass the subject, it is necessary that:

- The global mark of the theory (TM) is greater or equal than 4 over 10.
- The global mark of the laboratory (LM) is greater or equal than 4 over 10.
- The global mark of the subject (FM) is greater or equal than 5 over 10.

The laboratory mark is calculated as follows:

$$LM = (10/6) * (0,10 * LAP1 + 0,15 * LAP2 + 0,15 * LAP3 + 0,20 * LAP4)$$

being:

LAP<sub>i</sub> = Laboratory Autonomous Projects mark over 10.

In case a student passes all the minimum marks, the final mark (FM) will be:

$$FM = 0.40 * TM + 0.60 * LM$$

In case a student does not reach any of the minimum marks (theory mark < 4 or global laboratory mark < 4), the final mark (FM) will be:

$$FM = \text{minimum} [4.9; (0.40 * TM + 0.60 * LM)]$$

The students that pass the course by means of continuous assessment will not be allowed to repeat any tasks (theory, laboratory) in the global assessment in order to improve the mark.

If the students who are following continuous assessment deliver all the tasks, the mark of the part of the subject (theory, laboratory) in which they have obtained the minimum demanded will be preserved, only until the extraordinary exam of the same academic course.

### **GLOBAL ASSESSMENT (ordinary and extraordinary exam) and END-OF-PROGRAM EXAM**

The students that opt for the global assessment (whether it is the ordinary or extraordinary exam) or for the end-of-program exam will have to do a theoretical exam and a laboratory exam individually.

To be allowed to do the laboratory exam, it is necessary to request it previously on the dates that will be communicated to the students through the Moovi website.

The total mark will be the weighted sum of the marks obtained in the different tasks of the subject.

To pass the subject, it is necessary that:

- The mark of the theoretical exam (TE) is greater or equal to 4 over 10.
- The mark of the laboratory exam (LE) is greater or equal to 4 over 10.
- The global mark of the subject (FM) is greater or equal to 5 over 10.

In case a student passes all the different tasks, the final mark (FM) will be the weighted sum of the marks of each exam:

$$FM = 0.40 * TE + 0.60 * LE$$

In case a student does not pass one of the exams (theoretical exam < 4 or laboratory exam < 4), the final mark (FM) will be:

$$FM = \text{minimum} [4.9; (0.40 * TE + 0.60 * LE)]$$

#### **Theoretical exam**

The theoretical exam will include test questions and practical problems on the topics of all the theoretical lessons. The students will have to answer all the exam questions correctly to obtain the maximum mark.

This exam will be held on the date and place that the faculty will determine.

#### **Laboratory exam**

The exam will consist of the design of circuits in VHDL and programs for the microprocessor used in the subject. These circuits and programs may be part of a complex peripheral or an embedded system and they will have a similar complexity to the ones designed in the laboratory practical and the autonomous laboratory projects during the continuous assessment.

The students will have to perform the simulations and tests described in the exam in the assigned time.

The teacher may request that the students show them the operation of each of the circuits and programs.

All the sections have to work perfectly to obtain the maximum mark.

The addition of additional functionality to the minimum required will be taken into account.

It is compulsory to deliver the files indicated in the exam.

If this condition is not fulfilled, the corresponding sections will not be assessed.

The correct operation and the correct application of the theoretical concepts to the circuits and programs realised during the exam will be assessed, according to the same assessment criteria for the laboratory practices and the autonomous projects during the continuous assessment.

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### **Sources of information**

#### **Basic Bibliography**

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POZA GONZÁLEZ, F., ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño de sistemas empotrados de 8 bits en FPGAs con Xilinx ISE y Picoblaze**, Vision libros, 2012

Chu, Pong P., **FPGA prototyping by VHDL examples**, John Wiley & Sons, Inc., 2008

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### **Complementary Bibliography**

ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño Digital con FPGAs**, Vision libros, 2013

ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño Digital con Lógica Programable**, Editorial Tórculo, 2004

ÁLVAREZ RUIZ DE OJEDA, L. Jacobo, MANDADO PÉREZ, E., VALDÉS PEÑA, M.D., **Dispositivos Lógicos Programables y sus aplicaciones**, Editorial Thomson-Paraninfo, 2002

PÉREZ LÓPEZ, S.A., SOTO CAMPOS, E., FERNÁNDEZ GÓMEZ, S., **Diseño de sistemas digitales con VHDL**, Thomson-Paraninfo, 2002

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### **Recommendations**

#### **Subjects that continue the syllabus**

Application Design with micro-controllers/V05G301V01406

Design and synthesis of digital systems/V05G301V01408

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#### **Subjects that are recommended to be taken simultaneously**

Electronic Systems for Signal Processing/V05G301V01312

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#### **Subjects that it is recommended to have taken before**

Informatics: Computer Architecture/V05G301V01109

Digital electronics/V05G301V01203

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#### **Other comments**

The students will have previously followed the subject Digital Electronics. It gives the necessary knowledge to understand the topics of this course.

Besides, it is recommended that the students have previously followed the subject Informatics: Computer Architecture. It gives the necessary knowledge to understand some topics of this course.

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