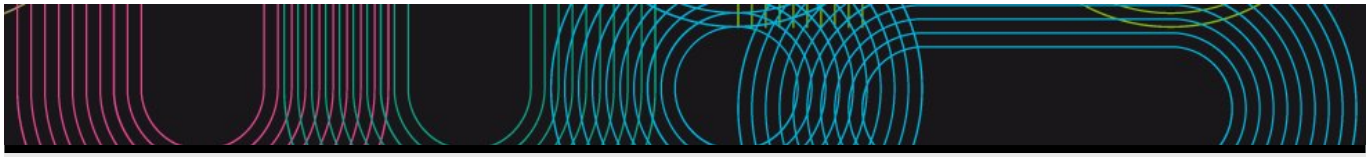
Universidade Vigo

Subject Guide 2024 / 2025



IDENTIFYING DATA				
Design and synthesis of digital systems				
Subject	Design and synthesis of digital systems			
Code	V05G301V01408			
Study programme	Grado en Ingeniería de Tecnologías de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Optional	4th	1st
Teaching language	English			
Department				
Coordinator	Álvarez Ruiz de Ojeda, Luís Jacobo			
Lecturers	Álvarez Ruiz de Ojeda, Luís Jacobo			
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General description	This course will be taught and assessed in English. The course documentation is in English. The main learning goals of this course are: □ Introduction to VHDL for synthesis. □ Design and synthesis of synchronous digital systems. □ Development, synthesis and verification of programmable digital circuits, using VHDL for its application in the field of the Telecommunications.			

Training and Learning Results	
Code	
B1	CG1: The ability to write, develop and sign projects in the field of Telecommunication Engineering, according to the knowledge acquired as considered in section 5 of this Law, the conception and development or operation of networks, services and applications of Telecommunication and Electronics.
B9	CG9: The ability to work in multidisciplinary groups in a Multilanguage environment and to communicate, in writing and orally, knowledge, procedures, results and ideas related with Telecommunications and Electronics.
B13	CG13 The ability to use software tools that support problem solving in engineering.
C62	(CE62/OP5) The ability to design and synthesize complex digital systems by hardware description language.
D4	CT4 Encourage cooperative work, and skills like communication, organization, planning and acceptance of responsibility in a multilingual and multidisciplinary work environment, which promotes education for equality, peace and respect for fundamental rights.

Expected results from this subject	Training and Learning Results		
To be able to distinguish the differences between the use of Hardware Description Languages for simulation and for synthesis.	B13	C62	
To deepen the understanding of synchronous digital design techniques using VHDL for synthesis.	B13	C62	
To acquire skills at designing complex synchronous digital systems using VHDL.	B1 B9 B13	C62	D4

Contents	
Topic	
LESSON 1 THEORY. INTRODUCTION TO COMPLEX DIGITAL SYSTEM DESIGN AND SYNTHESIS.	1.1.- Introduction. 1.2.- Complex application specific digital system design by means of FPGAs. 1.2.1.- Sequential processing systems. 1.2.2.- Continuous processing systems.

LESSON 2 THEORY. DIGITAL SYSTEM DESIGN RULES.	2.1.- Introduction. 2.2.- General rules for the design of digital systems. 2.2.1.- Hierarchical design. 2.2.2.- Technology independent design. 2.2.3.- Design timing. 2.2.4.- Design for reuse. 2.2.5.- Design for verificability. 2.2.6.- Design documentation. 2.3.- Intellectual Property (IP) cores.
LESSON 3 THEORY. INTRODUCTION TO SYNTHESIS OF DIGITAL SYSTEMS DESCRIBED IN VHDL.	3.1.- Introduction. 3.2.- Definition of synthesis. Basic concepts on synthesis. 3.3.- Conversion of a VHDL description to real hardware. Differences between the original VHDL model and the result of the synthesis / implementation. Timing simulation model. 3.4.- Recommendations for the description in VHDL synthesisable of distinct types of circuits. 3.5.- Examples of synthesisable models of commonly used circuits.
LESSON 4 THEORY. VHDL ADVANCED SENTENCES.	4.1.- Introduction. 4.2.- Access to files. 4.2.1.- Memory initialisation. 4.2.2.- Testbench stimuli. 4.3.- Generic data type. Parameterisable circuits. 4.4.- Libraries and packages. 4.5.- Subprograms. 4.5.1.- Functions. 4.5.2.- Procedures. 4.6.- Conditional compilation.
LESSON 5 THEORY. VHDL FOR SYNTHESIS. RESTRICTIONS.	5.1.- Introduction. 5.2.- IEEE standard for synthesis. 5.3.- Time sentences (After, Wait). 5.4.- Loops (Loop). Loops generate. 5.5.- Real data type. Type conversion. 5.6.- Complex arithmetical operations. Division (/). 5.7.- Complex mathematical functions. (Without, Cos, Log). 5.8.- Two-dimensional matrices. (Array). 5.9.- Exercises of non- synthesisable models and equivalent synthesisable circuits.
LESSON 6 THEORY. ARITHMETICAL CIRCUITS DESIGN IN VHDL.	6.1.- Introduction. 6.2.- Representation of binary numbers with decimal part. Fixed point. Floating point. 6.3.- Design of fixed point applications. 6.4.- Design of floating point applications. 6.5.- Implementation of arithmetical circuits in FPGAs.
LESSON 7 THEORY. VERIFICATION OF COMPLEX DIGITAL SYSTEMS.	7.1.- Introduction. 7.2.- Verification through simulation. 7.2.1.- Signals. Delay models. Definition of □driver□. 7.2.2.- Design analysis and simulation. Simulation cycle. Delta delay. 7.2.3.- Recommendations for VHDL simulation. Examples. Testbench design. 7.2.4.- Differences between functional and timing simulation. 7.3.- Verification through timing analysis. 7.4.- Verification through test in a development board. 7.5.- Exercises.
LESSON 1 LABORATORY. PRACTICAL TUTORIAL OF DIGITAL SYSTEM DESIGN AND SYNTHESIS.	1.1.- Introduction. 1.2.- Basic digital system design in synthesisable VHDL. 1.3.- Testbench design in VHDL. 1.4.- Implementation of digital systems in FPGAs. 1.5.- Testing digital systems.
LESSON 2 LABORATORY. DESIGN OF A MEDIUM-COMPLEXITY DIGITAL SYSTEM IN SYNTHESISABLE VHDL.	2.1.- Introduction. Task explanation. (2 h. TYPE B) 2.2.- Project based learning. Discussions on the most suitable approach. (6 h. TYPE C) 2.2.- Design of a medium-complexity digital system in synthesisable VHDL. (6 h. TYPE B) 2.3.- Oral presentation. (1 h. TYPE C)

Planning			
	Class hours	Hours outside the classroom	Total hours

Lecturing	4	8	12
Project based learning	15	31.5	46.5
Laboratory practical	6	7.5	13.5
Project based learning	14	51	65
Presentation	1	8	9
Introductory activities	2	2	4

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies

	Description
Lecturing	Conventional lectures. Through this methodology the outcome C62 is developed.
Project based learning	Problem based learning (PBL): Problem solving. It will consist mainly of the design of non-synthesisable models and synthesisable circuits in VHDL. To solve them, the student has to previously develop certain outcomes. Through this methodology the outcomes B9, B13 and C62 are developed.
Laboratory practical	VHDL design of digital circuits and circuit implementation in FPGAs. Software to be used: Vivado Design Suite de Xilinx Through this methodology the outcomes B9, B13 and C62 are developed.
Project based learning	Project based learning. The students must design a digital system in VHDL to solve a problem. In order to do that, the students must plan, design and implement the necessary steps. The project development will be implemented in laboratory hours (type B). Besides, in type C hours there will be discussions and one-to-one interaction with the teacher. Activities to develop in the groups C: Analysis and debate about the project approach and different alternatives. Analysis and follow-up of the proposed solution. Design implementation. Analysis and debate of results. Oral presentations of the project results. Through this methodology the outcomes B1, B9, B13, D4 and C62 are developed.
Presentation	Presentations/exhibitions: Exhibition of the results of the project developed. Through this methodology the outcomes B1 and B9 are developed.
Introductory activities	Introduction to the subject key topics both theoretical and practical. Through this methodology the outcomes B13 and C62 are developed.

Personalized assistance

Methodologies	Description
Project based learning	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the following website: https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda
Laboratory practical	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the following website: https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda
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Assessment

	Description	Qualification	Training and Learning Results

Project based learning	Problem-based learning. The total mark will be the sum of the marks of each one of the weekly exercise reports divided by the number of reports: TE = (Report 1 + ... + Report N) / N The estimated number of reports is 10. Resolution of theoretical problems and exercises. The majority of them will be focused on the design of non-synthesisable models and synthesisable circuits in VHDL. The problems will be based on the theoretical topics. It will be necessary to teach to the professor the operation of each one of the models and circuits. The correct application of the theoretical concepts to the problems will be assessed, based on the published criteria. It will be necessary to deliver the documentation requested by the professor for each one of the exercises.	40	B13	C62	
Laboratory practical	These practical exercises will consist of the development of circuits in a guided manner. The assessment will be based on the operation of the digital system, according to the published criteria.	10	B13	C62	
Project based learning	Laboratory Project. Design of a medium-complexity synthesisable digital system in VHDL. It will be necessary to deliver the design source files. The assessment will be based on the operation of the digital system and the correct application of the theoretical concepts, according to the published criteria.	40	B1 B9 B13	C62	D4
Presentation	It will be necessary to do an oral presentation of 15 minutes as a maximum about the work, according to the index supplied by the teacher.	10	B1 B9		D4

Other comments on the Evaluation

The total mark will be the sum of the marks obtained in the different tasks of the subject.

The global mark of the theoretical problems has to be equal or greater than 5 over 10 in order to pass the subject.

The mark of the Laboratory Project has to be equal or greater than 5 over 10 in order to pass the subject.

The students will be offered two assessment systems: continuous assessment and global assessment.

All the students, whether they follow the subject continuously or want to be assessed in the global assessment (ordinary or extraordinary call or end-of-program call), will have to do the tasks described in the previous section.

The students that do not attend classes regularly will also have to do the same tasks as the students who attend classes.

The final mark will be expressed in numerical form ranging from 0 to 10.

CONTINUOUS ASSESSMENT IN ORDINARY CALL

The students are considered to have chosen the continuous assessment when they have done 2 laboratory practices and/or 2 reports of theoretical exercises. However, it is possible to waive continuous assessment and opt for global assessment, upon a written request to the subject coordinator, within one month from the beginning of the semester.

The students that have chosen continuous assessment, but do not pass the course, will have to do the global assessment at the extraordinary opportunity.

The students that pass the course by means of continuous assessment will not be allowed to repeat any task in the global assessment in order to improve the mark.

The different tasks should be delivered in the date specified by the teacher, otherwise they will not be assessed for the continuous assessment.

The students will develop the theoretical exercises and the laboratory practices individually.

The laboratory projects will be developed in groups of two students during the continuous assessment but the students will be assessed individually. To achieve this, the students will be required to explain during the oral presentation which parts of the project each of them has developed.

The students who want to be assessed in the continuous assessment can only miss two sessions as a maximum. If they miss more than 2 sessions, it will be compulsory to do an additional individual task or an examination.

GLOBAL ASSESSMENT (ordinary or extraordinary call) and END-OF-PROGRAM CALL

The students that opt for the global assessment (whether it is at the ordinary or extraordinary call) or for the end-of-program call will have to do all the theoretical and practical tasks and the project individually.

The tasks for the single assessment must be delivered before the official date of the examination set by the faculty.

FINAL MARK OF THE COURSE

In case the students pass the theoretical exercises (TE) and the Laboratory Project (LP), that is, the mark of each part >= 5,

the final mark (FM) will be the weighted sum of the marks of each part of the subject:

FM = 0,40 * TE + 0,10 * Lp + 0,40 * LP + 0,10 * OP

Where:

TE = Global mark of the theoretical exercises and problems.

Lp = Laboratory Practices.

LP = Laboratory Project.

OP = Oral presentation.

In case the students have a final mark greater or equal than 5 but have not passed any of the two main parts of the subject, the theoretical exercises (TE) or the Laboratory Project (LP), that is, the mark of any part < 5, the final mark (FM) will be 4.9.

Theoretical exercises and problems

Each one of the theoretical exercises and problems proposed in the theoretical sessions will be marked from 0 to 10. Its influence in the total mark of the subject will be weighted in function of the number of exercises assigned.

The majority of the exercises will consist in the design of non-synthesisable models and synthesisable circuits in VHDL.

It will be necessary to deliver the required source files.

The total mark will be the sum of the marks of each one of the exercise reports divided by the number of reports:

TE = (Report 1 + ... + Report N) / N

The estimated number of reports is 10.

Plagiarism is regarded as serious dishonest behavior. If any form of plagiarism is detected in any of the exercises, the final mark will be FAIL (0), and the incident will be reported to the corresponding academic authorities for appropriate action

Sources of information

Basic Bibliography

CHU, PONG P., **RTL Hardware Design Using VHDL: Coding for Efficiency,Portability, and Scalability**, John Wiley & Sons Inc, 2006

ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño Digital con FPGAs**, Visión libros, 2013

Complementary Bibliography

ASHENDEN, PETER J., **The Designer's Guide to VHDL**, 3, MorganKaufmann Publishers, 2008

Standard IEEE VHDL Language Reference Manual (IEEE Srd 1076-2001), IEEE, 2001

CHU, PONG P., **FPGA Prototyping by VHDLExamples**, John Wiley & Sons Inc, 2008

Recommendations

Subjects that it is recommended to have taken before

Digital electronics/V05G301V01203
Programmable Electronic Circuits/V05G301V01302
Electronic Systems for Signal Processing/V05G301V01312

Other comments

The students will have previously followed the subjects Digital Electronics and Programmable Electronic Circuits. They give the necessary knowledge to understand the topics of this course.
It is not necessary to have passed them.

The students of the specialisation Electronic Systems, should have previously followed the subject Electronic Systems for Signal Processing, but it is not indispensable.