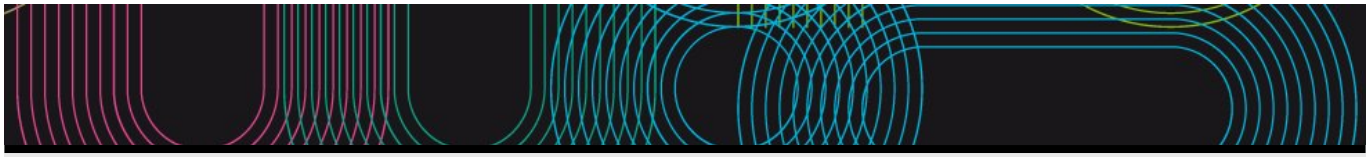

IDENTIFYING DATA				
Hardware/Software Design of Embedded Systems				
Subject	Hardware/Software Design of Embedded Systems			
Code	V05M145V01214			
Study programme	Máster Universitario en Ingeniería de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	5	Optional	1st	2nd
Teaching language	Spanish Galician English			
Department				
Coordinator	Álvarez Ruiz de Ojeda, Luís Jacobo Machado Domínguez, Fernando			
Lecturers	Álvarez Ruiz de Ojeda, Luís Jacobo			
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General description	This course will be taught and assessed in English. The documentation of the subject will be in English. The main learning goals of this course are: - To learn the codesign methods to design applications based on embedded microprocessors in FPGAs. - To get to know the microprocessors that can be implemented in commercial FPGAs. - To handle the necessary software tools for the development of embedded applications by means of FPGAs. - To design application specific peripherals and their connection to the buses of the embedded microprocessors. - To design real digital applications with embedded microprocessors in FPGAs.			

Training and Learning Results	
Code	
A5	CB5 Students must have learning skills to allow themselves to continue studying in largely self-directed or autonomous way
B1	CG1 Ability to project, calculate and design products, processes and facilities in telecommunication engineering areas.
B8	CG8 Ability to apply acquired knowledge and to solve problems in new or unfamiliar environments within broader and multidiscipline contexts, being able to integrate knowledge.
C11	CE11 Knowledge of hardware description languages for high complexity circuits.
C12	CE12 Ability to use programmable logic devices, as well as to design advanced electronic systems, both analog and digital. The ability to design communications components such as routers, switches, hubs, transmitters and receivers in different bands.

Expected results from this subject	
Expected results from this subject	Training and Learning Results
To learn the codesign methods to design applications based on embedded microprocessors in FPGAs.	A5 C11 C12
To get to know the microprocessors that can be implemented in commercial FPGAs.	A5 C11 C12
To handle the necessary software tools for the development of embedded applications by means of FPGAs.	A5 C11 C12

To design application specific peripherals and their connection to the buses of the embedded microprocessors.	A5 B1 B8 C11 C12
To design real applications with embedded microprocessors in FPGAs.	A5 B1 B8 C11 C12

Contents	
Topic	
LESSON 1 THEORY. INTRODUCTION TO THE DESIGN OF EMBEDDED SYSTEMS. (1 h.)	1.1. Introduction. 1.2. Programmable Systems On Chip (PSOC). 1.3. Hardware/Software Codesign. Codesign phases. 1.4. Xilinx SOC Zynq family introduction. 1.5. Xilinx Vivado and SDK tools for codesign of embedded systems.
LESSON 2 THEORY. MICROPROCESSOR OF THE XILINX ZYNQ FAMILY SOCs. (0.5 h.)	2.1. ARM processor from Zynq SOC family (Zynq Processing Systems (PS)). 2.2. Processor peripherals from Zynq SOC family. 2.3. Clock, reset and processor debugging. 2.4. AXI interface.
LESSON 3 THEORY. FPGA OF THE XILINX ZYNQ FAMILY SOCs. (0.5 h.)	3.1. Introduction to 7 series Xilinx FPGAs. 3.1.1. Logic resources. 3.1.2. Input/output resources. 3.1.3. Memory and signal processing resources. 3.1.4. Analog to digital converter. 3.1.5. Clock resources.
LESSON 4 THEORY. CONNECTION OF PERIPHERAL CIRCUITS TO THE XILINX ARM MICROPROCESSOR. (1 h.)	4.1.- Introduction. 4.2.- Interface for basic peripherals. GPIO. 4.3.- Interface for advanced peripherals. IPIF. 4.4.- Interface for user coprocessors
LESSON 5 THEORY. SOFTWARE DEVELOPMENT FOR THE XILINX ARM MICROPROCESSOR. (1 h.)	5.1.- Introduction. 5.2.- Structure of the routines for handling of peripherals. 5.3.- Interrupt handle. 5.4.- Program debugging.
LESSON 6 THEORY. HARDWARE / SOFTWARE PARTITIONING. (1 h.)	6.1.- Introduction. 6.2.- Examples of hardware / software codesign. 6.3.- Distribution of tasks between hardware and software.
LESSON 7 THEORY. EMBEDDED SYSTEMS ANALISYS PROJECT. (5 h.)	7.1. Design of a software routine for the assigned function. 7.2. Design of a hardware peripheral (coprocessor) for the assigned function. 7.3. Profiling analysis from software routine and hardware peripheral. Comparison of results.
LESSON 1 LABORATORY. XILINX VIVADO ENVIRONMENT FOR THE DESIGN OF EMBEDDED SYSTEMS. (1.5 h.)	1.1. Introduction. 1.2. Xilinx Vivado environment. 1.3. Design of basic examples of embedded systems. 1.3.1. Addition of predefined peripherals (IP cores). 1.4. Implementation of the developed systems in Digilent evaluation boards.
LESSON 2 LABORATORY. DESIGN OF BASIC PERIPHERAL CIRCUITS. (2 h.)	2.1. Introduction. 2.2. Development of basic user peripherals. GPIO.
LESSON 3 LABORATORY. DESIGN OF ADVANCED PERIPHERAL CIRCUITS. (1.5 h.)	3.1. Introduction. 3.2. Development of advanced user peripherals (Custom IP).
LESSON 4 LABORATORY. XILINX SDK ENVIRONMENT FOR THE DESIGN OF EMBEDDED SYSTEMS SOFTWARE. (1 h.)	4.1. Introduction. 4.2. Xilinx Software Development Kit (SDK) environment. 4.3. Basic Design Examples.
LESSON 5 LABORATORY. SOFTWARE DEBUGGING OF EMBEDDED APPLICATIONS. (1 h.)	5.1. Introduction. 5.2. Software debugging of embedded systems by means of the GNU debugger from SDK.
LESSON 6 LABORATORY. HARDWARE VERIFICATION OF EMBEDDED APPLICATIONS. (1.5 h.)	6.1. Introduction. 6.2. Embedded systems hardware verification using Vivado hardware analyzer.
LESSON 7 LABORATORY. EMBEDDED SYSTEMS PROFILING. (1.5 h.)	7.1. Introduction. 7.2. Software profiler.

LESSON 8 LABORATORY. DESIGN PROJECT. DESIGN OF AN APPLICATION BASED IN XILINX 32-BIT MICROPROCESSORS. (10 h.: 5 h. type B + 5 h. type C)	8.1. Design and test of the assigned application.

Planning			
	Class hours	Hours outside the classroom	Total hours
Lecturing	5	10	15
Problem solving	5	20	25
Laboratory practical	10	10	20
Mentored work	9	48	57
Presentation	1	7	8

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies	
	Description
Lecturing	Conventional lectures. Through this methodology the outcomes C11 and C12 are developed.
Problem solving	Problem based learning (PBL): Problem solving. Design of synthesizable circuits in VHDL and software programs in C language. To solve them, the student has to previously develop certain outcomes. Through this methodology the outcomes A5, B1, B8, C11 and C12 are developed.
Laboratory practical	VHDL design of digital circuits and circuit implementation in FPGAs and development of software programs in C language. Integration of both to build an embedded system in a FPGA. Software to be used: Vivado Design Suite from Xilinx. Through this methodology the outcomes A5, B8, C11 and C12 are developed.
Mentored work	Project based learning. The students must design an embedded system to solve a problem. In order to that, the students must plan, design and implement the necessary steps. Through this methodology the outcomes A5, B1, B8, C11 and C12 are developed
Presentation	Exhibition of the results of the project developed. Through this methodology the outcomes A5, C11 and C12 are developed.

Personalized assistance	
Methodologies	**Description**
Lecturing	In class, the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours, which will be published in the following website: https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda
Laboratory practical	In class, the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours, which will be published in the following website: https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda
Problem solving	In class, the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours, which will be published in the following website: https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda
Mentored work	In class, the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours, which will be published in the following website: https://www.uvigo.gal/es/universidad/administracion-personal/pdi/luis-jacobo-alvarez-ruiz-ojeda

Assessment				
	Description	Qualification	Training and Learning Results	
Problem solving	Problem Based Learning. Resolution of exercises and theoretical problems. The correct application of the theoretical concepts to the problems will be assessed, based on the published criteria.	25	A5 	B1 C11 B8 C12

Laboratory practical	Design circuits and programs in the laboratory sessions corresponding to the laboratory lessons 1 to 7. It will be necessary to show to the professor the operation of each one of the circuits and programs. It will be necessary to deliver the design source files. The assessment will be based on the operation of the digital system and the correct application of the theoretical concepts, according to the published criteria.	25	A5	B8	C11 C12
Mentored work	Project Based Learning. Laboratory Project. Design of an embedded system. It will be necessary to deliver the files source of the work realized. It will be necessary to deliver the design source files. The assessment will be based on the operation of the embedded system and the correct application of the theoretical concepts, according to the published criteria.	40	A5	B1 B8	C11 C12
Presentation	It will be necessary to do an oral presentation of 15 minutes as a maximum about the work, according to the index supplied by the teacher.	10	A5		C11 C12

Other comments on the Evaluation

The final mark will be expressed in numerical form ranging from 0 to 10, according to the valid regulation (Royal decree 1125/2003 of 5 September; BOE 18 September).

Following the guidelines of the degree the students will be offered two evaluation systems: continuous assessment and global assessment. Students must choose at the start of the subject if they wish to follow the continuous evaluation or prefer to follow the global assessment at the end of the semester. Students who choose global assessment must notify the subject coordinator in writing within one month from the beginning of the semester.

CONTINUOUS ASSESSEMENT IN ORDINARY CALL

The students that have chosen continuous assessment, but do not pass the course, will have to do the global assessment in extraordinary call.

The different tasks should be delivered in the date specified by the teacher, otherwise they will not be assessed for the continuous evaluation.

If the number of students allows it, the students will develop the theoretical exercises, the laboratory practices and the laboratory projects individually. In case of doing them in groups of two students the mark will be the same for both.

The students who want to be assessed in the continuous evaluation can only miss two sessions of any type as a maximum. If they miss more than 2 sessions, it will be compulsory to do an additional individual task or an examination.

1) Laboratory practices.

Each laboratory practice will be marked from 0 to 10. Its influence in the total mark of the subject will be weighted in function of the number of hours assigned to each lesson. That is, the mark of the practices will be obtained through the following formula:

LAB = Mark Lesson 1L + ... + Mark Lesson 7L

2) Theoretical exercises and problems.

Each one of the theoretical exercises and problems proposed in the theoretical sessions will be evaluated. Each exercise will be marked from 0 to 10. Its influence in the total mark of the subject will be weighted according to the difficulty and length of the exercise.

The main exercise will consist in the design of a software routine and a hardware peripheral to perform the function assigned to each student and compare the performance of both, in terms of execution time and logical resources used. The content corresponds to topic 7 of theory. It will be necessary to show the teacher the operation of each one of the circuits and programs. It will be necessary to deliver a brief report explaining the work done.

The total mark will be the sum of the marks of each one of the exercises:

TE = Exercise 1 + ... + Exercise N

3) Tutored works.

This work consists in the design of an embedded system. The correct operation of the developed circuits and programs will

be evaluated. This work will be marked from 0 to 10.

4) Presentation.

The work developed during the laboratory project will be presented. The presentation will be marked from 0 to 10.

In case the students pass the theoretical exercises (TE), the laboratory practices (LAB) and the tutored works (TW), that is, the mark of each part >= 5, the final mark (FM) will be the weighted sum of the marks of each part of the subject:

FM = 0,25 * TE + 0,25 * LAB + 0,40 * TW + 0,10 * OP

In case the students do not pass any of the three main parts of the subject, that is, the mark of any task < 5, the final mark (FM) will be:

FM = Minimum [4'9; (0,25 * TE + 0,25 * LAB + 0,40 * TW + 0,10 * OP)]

Where:

TE = Global mark of the theoretical exercises and problems.

LAB = Laboratory Practices.

TW = Tutored Work.

OP = Oral presentation.

GLOBAL ASSESSMENT(ordinary or extraordinary call) AND END-OF-PROGRAM CALL

The students that opt for the global assessment in ordinary call or do not pass the subject and have to do the global assessment in the extraordinary call must do an exam, which will be divided into two parts: a theoretical part and a practical part.

The theoretical part will consist in the design of a peripheral with a certain functionality that has an AXI-Lite interface, which allows its connection to a Microprocessor. The mark will be from 0 to 10 and its weight in the final grade will be 40%.

The practical part will consist in the design of a embedded system with the necessary peripherals to perform a certain task. The mark will be from 0 to 10 and its weighting in the final grade will be 60%.

In case the students pass each part, that is, the mark of each part >= 5, the final mark (FM) will be the weighted sum of the marks of each part:

NF = 0,40 * TE + 0,60 * PE

In case the students do not pass any of the parts of the exam, that is, the mark of any part < 5, the final mark (FM) will be:

NF = minimum [4,9; (0,40 * TE + 0,60 * PE)]

Where:

TE = Global mark of the theoretical part.

PE = Global mark of the practical part.

Plagiarism is regarded as serious dishonest behavior. If any form of plagiarism is detected in any of the exercises, the final mark will be FAIL (0), and the incident will be reported to the corresponding academic authorities for appropriate action.

Sources of information

Basic Bibliography

ÁLVAREZ RUIZ DE OJEDA, L.J., POZA GONZÁLEZ, F., **Diseño de aplicaciones empotradas de 32 bits en FPGAs con Xilinx EDK 10.1 para Microblaze y Power-PC**, Vison Libros,

Complementary Bibliography

ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño Digital con FPGAs**, Vision Libros,

Recommendations

Subjects that are recommended to be taken simultaneously

Advanced Digital Electronic Systems/V05M145V01203