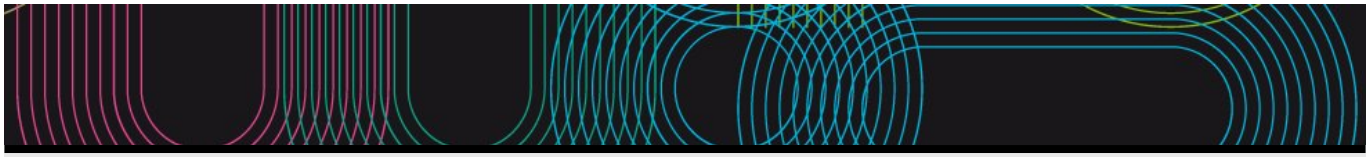

IDENTIFYING DATA				
Programmable Electronic Circuits				
Subject	Programmable Electronic Circuits			
Code	V05G300V01502			
Study programme	Degree in Telecommunications Technologies Engineering - In extinction			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Mandatory	3rd	1st
Teaching language	Spanish Galician			
Department				
Coordinator	Poza González, Francisco			
Lecturers	Álvarez Ruiz de Ojeda, Luís Jacobo Costas Pérez, Lucía Poza González, Francisco Valdés Peña, María Dolores			
E-mail	fpoza@uvigo.es			
Web	http://www.faitic.uvigo.es/			
General description	Part of the documentation of the subject is in English. The objectives of this course are that students learn the general aspects of the architecture of microprocessors, microcontrollers and configurable devices, as well as the adequate design methods and tools, while they acquire the necessary skills to design systems based on these devices.			

Competencies	
Code	
B3	CG3: The knowledge of basic subjects and technologies that enables the student to learn new methods and technologies, as well as to give him great versatility to confront and adapt to new situations
B4	CG4: The ability to solve problems with initiative, to make creative decisions and to communicate and transmit knowledge and skills, understanding the ethical and professional responsibility of the Technical Telecommunication Engineer activity.
B13	CG13 The ability to use software tools that support problem solving in engineering.
C7	CE7/T2: The ability to use communication and software applications (ofimatics, databases, advanced calculus, project management, visualization, etc.) to support the development and operation of Electronics and Telecommunication networks, services and applications.
C8	CE8/T3: The ability to use software tools for bibliographical resources search or information related with electronics and telecommunications.
C14	CE14/T9: The ability to analyze and design combinatory and sequential, synchronous and asynchronous circuits and the usage of integrated circuits and microprocessors.
C15	CE15/T10: The knowledge and application of the fundamentals of description languages for hardware devices.
D2	CT2 Understanding Engineering within a framework of sustainable development.
D3	CT3 Awareness of the need for long-life training and continuous quality improvement, showing a flexible, open and ethical attitude toward different opinions and situations, particularly on non-discrimination based on sex, race or religion, as well as respect for fundamental rights, accessibility, etc.

Learning outcomes		
Expected results from this subject		Training and Learning Results
New		
To understand the basic architecture of microprocessors, microcontrollers and configurable devices (FPGAs).	B3	C14 C15
To know the methods and techniques of design of integrated hardware/software systems (System on Chip □ SoC).	B3	C14 C15

To know the hardware and software tools for the design of systems based in programmable devices.	B13	C14 C15	
To acquire the skills to use the design tools for the design of digital systems.		C14 C15	
Ability to design simple integrated systems (System on Chip □ SoC) applied to the telecommunications fields.	B3 B4 B13	C7 C8 C14 C15	D2 D3

Contents	
Topic	
LESSON 0 THEORY (2 h.). REVIEW OF DIGITAL CIRCUITS.	0.1.- Digital circuits. 0.1.1.- Combinational circuits. 0.1.2.- Aritmetic circuits. 0.1.3.- Sequential circuits. 0.2.- VHDL. 0.2.1.- VHDL syntax. 0.2.2.- VHDL sentences.
LESSON 1 THEORY (5 h.). DESIGN OF COMPLEX SYSTEMS.	1.1.- Introduction. 1.2.- Previous analysis of the most suitable solution. 1.3.- Application specific peripherals. Design methods. 1.3.1.- Practical examples.
LESSON 2 THEORY (1 h.). INTRODUCTION TO CORRECT DESIGN METHODS.	2.1.- Introduction. 2.2.- Design of digital systems with FPGAs. 2.2.1.- Hierarchical design. 2.2.2.- Technology-independent design. 2.2.3.- Timing design.
LESSON 3 THEORY (2 h.). SYNCHRONOUS DIGITAL SYSTEM DESIGN.	3.1.- Introduction. 3.2.- Synchronous design. 3.3.- Synchronous sequential systems. FPGA design recommendations. 3.4.- Synchronisation of input variables.
LESSON 4 THEORY (2 h.). XILINX PICOBLAZE MICROPROCESSOR (I).	4.1.- Introduction. 4.2.- Versions of the Xilinx Picoblaze microprocessor. 4.3.- Internal architecture of the Picoblaze microprocessor. 4.4.- Instruction set of the Picoblaze microprocessor.
LESSON 5 THEORY (1 h.). SOFTWARE DEVELOPMENT FOR XILINX PICOBLAZE MICROPROCESSOR.	5.1.- Introduction. 5.2.- Syntax of an assembler program for the Picoblaze microprocessor. 5.3.- Program development with pBlazeIDE environment for Picoblaze .
LESSON 6 THEORY (4 h.). XILINX PICOBLAZE MICROPROCESSOR (II).	6.1.- Introduction. 6.2.- External architecture. 6.2.1.- Input / Output instructions. 6.2.2.- Connection of input peripherals. 6.2.3.- Connection of output peripherals. 6.2.4.- Picoblaze reset. 6.2.5.- External interrupts. 6.3.- Design of peripherals for the Picoblaze microprocessor.
LESSON 7 THEORY (1 h.). INTRODUCTION TO FPGAs.	7.1.- Introduction. 7.2.- Definition of FPGA. FPGA classification. 7.3.- FPGA architectures. 7.3.1.- Logical resources. 7.3.2.- Interconnection resources. 7.3.3.- Examples of commercial FPGAs. 7.4.- FPGA technologies. 7.5.- General characteristic of the FPGAs. 7.6.- Advantages of the FPGAs. 7.7.- FPGA design flow. 7.7.1.- Design implementation with FPGAs. 7.8.- FPGA CAD tools. 7.9.- FPGA applications.
LESSON 8 THEORY (1 h.). XILINX ARTIX 7 FPGA FAMILY. ARCHITECTURE.	8.1.- Introduction. 8.2.- Xilinx Artix 7 family architecture. 8.2.1.- Logical resources. CLBs. □Slices□. RAM-based shift registers. 8.2.2.- Internal memories. Distributed memory. Embedded memory. 8.2.3.- Clock circuits. 8.2.4.- DSP circuits. 8.2.5.- Input / Output technologies.

LESSON 9 THEORY (2 h.). INTRODUCTION TO MICROCONTROLLERS.	9.1.- Introduction. Definition of microcontroller. 9.2.- Internal architecture. Harvard. Von Neumann. 9.3.- External architecture. 9.4.- Integrated peripherals. 9.5.- Examples of commercial microcontrollers. 9.6.- Microcontroller applications. 9.7.- Tools for programming and verification.
LESSON 10 THEORY (1 h.). INTRODUCTION TO SYSTEMS ON CHIP (SOC).	10.1.- Introduction to digital design methods. 10.1.1.- Software method. 10.1.2.- Hardware method. 10.2.- Systems On Chip (SOC). 10.3.- Systems On a Programmable Chip (PSOC). Microprocessors embedded in FPGAs. 10.3.1.- Hardware Microprocessors. 10.3.2.- Software Microprocessors. 10.4.- Embedded microprocessor applications.
LESSON 11 THEORY (4 h.). HARDWARE / SOFTWARE CODESIGN.	11.1.- Introduction. 11.2.- Hardware / software codesign. 11.3.- Examples of hardware / software codesign.
LESSON 1 LABORATORY (2 h.). INTRODUCTION TO DESIGN WITH FPGAs	1.1.- Introduction to the digital systems design tool with FPGAs. 1.2.- Digital system description. 1.3.- Simulation. 1.4.- Synthesis and implementation. 1.5.- FPGA based development board. 1.6.- FPGA programming. 1.7.- Exercises.
LESSON 2 LABORATORY (8 h.). PROJECTS. DESIGN OF PERIPHERALS FOR THE PICOBLAZE MICROPROCESSOR.	2.1.- Design and implementation of a medium-complexity peripheral for the Picoblaze 3 microprocessor, according to the instructions supplied by the teacher through FaiTIC website.
LESSON 3 LABORATORY (2 h.). XILINX PICOBLAZE MICROPROCESSOR SOFTWARE TOOLS.	3.1.- Introduction. 3.2.- Program assembler and simulator in Mediatronix. Picoblaze IDE. 3.3.- Exercises.
LESSON 4 LABORATORY (6 h.). DESIGN OF DIGITAL SYSTEMS BASED ON THE PICOBLAZE MICROPROCESSOR.	4.1.- Introduction to the design of embedded systems. 4.2.- Design flow for embedded systems in FPGAs. 4.3.- Microprocessor program design. 4.4.- Description of the necessary hardware circuits. 4.5.- Program and hardware simulation. 4.6.- Test of the complete digital system. 4.7.- Design of a basic example with use of interrupts, based on the Picoblaze microprocessor.
LESSON 5 LABORATORY (8 h.). PROJECTS. DESIGN OF AN EMBEDDED SYSTEM BASED ON THE PICOBLAZE MICROPROCESSOR.	5.1.- Design and implementation of a medium-complexity application example based on the Picoblaze 3 microprocessor, according to the instructions supplied by the teacher through FaiTIC website.

Planning

	Class hours	Hours outside the classroom	Total hours
Introductory activities	2	2	4
Lecturing	12	16	28
Problem solving	12	19	31
Laboratory practical	10	12	22
Mentored work	16	32	48
Objective questions exam	1	3	4
Problem and/or exercise solving	3	10	13

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies

	Description
Introductory activities	Introduction to key topics both theoretical and practical. Through this methodology the outcome CG3 is developed.
Lecturing	Conventional lectures. Through this methodology the outcome CG3 is developed.
Problem solving	In these sessions, exercises will be solved by both the teacher and the students. Through this methodology the outcomes CG3, CG4, CE8/T3, CE14/T9 and CE15/T10 are developed.

Laboratory practical	In these sessions, both guided practices and exercises of circuits and programs will be set out. Through this methodology the outcomes CG3, CG4, CG13, CE7/TE2, CE8/T3, CE14/T9, CE15/T10, CT2 and CT3 are developed.
Mentored work	The students will have to develop two laboratory projects which consist of designing circuits and programs. These projects are related to laboratory lessons 2 and 5. Through this methodology the outcomes CG3, CG4, CG13, CE7/TE2, CE8/T3, CE14/T9, CE15/T10, CT2 and CT3 are developed.

Personalized assistance

Methodologies	Description
Introductory activities	Questions will be answered preferably via email, videoconference and forums on FaiTIC. If there are face-to-face classes, students' questions will also be answered during them. Moreover, students will have the opportunity to schedule an appointment to receive tuition in the place designated by the teachers, if that is possible.
Lecturing	Questions will be answered preferably via email, videoconference and forums on FaiTIC. If there are face-to-face classes, students' questions will also be answered during them. Moreover, students will have the opportunity to schedule an appointment to receive tuition in the place designated by the teachers, if that is possible.
Problem solving	Questions will be answered preferably via email, videoconference and forums on FaiTIC. If there are face-to-face classes, students' questions will also be answered during them. Moreover, students will have the opportunity to schedule an appointment to receive tuition in the place designated by the teachers, if that is possible.
Laboratory practical	Questions will be answered preferably via email, videoconference and forums on FaiTIC. If there are face-to-face classes, students' questions will also be answered during them. Moreover, students will have the opportunity to schedule an appointment to receive tuition in the place designated by the teachers, if that is possible.
Mentored work	Questions will be answered preferably via email, videoconference and forums on FaiTIC. If there are face-to-face classes, students' questions will also be answered during them. Moreover, students will have the opportunity to schedule an appointment to receive tuition in the place designated by the teachers, if that is possible.

Assessment

	Description	Qualification	Training and Learning Results		
Laboratory practical	The assessment will be based on the operation of the circuits and programs developed in the practical sessions corresponding to the laboratory lessons 1, 3 and 4, according to the published criteria. It will be necessary to show the teacher the operation of each of the circuits and programs.	20	B3 B4 B13	C7 C8 C14 C15	D2 D3
Mentored work	Autonomous Project. The students will have to develop two autonomous projects. The first project will consist of the design of a complex peripheral. The peripheral must be composed by a control unit and an ALU and must be designed following the method analysed in the theoretical lesson 1. The content corresponds with laboratory lesson 2. The second project will consist of the design of a medium-complexity embedded digital system. The embedded system must be composed by a microprocessor and its peripherals, as well as the auxiliary circuits needed to work correctly. It will also be necessary to develop a program for the microprocessor in assembler language. The content corresponds with laboratory lesson 5. In both projects the assessment will be based on the correct operation of the circuits and programs developed during the laboratory sessions assigned to the abovementioned lessons, as well as the correct application of the theoretical concepts to the work done, according to the published criteria. It will be necessary to show every circuit and program to the teacher.	30	B3 B4 B13	C7 C8 C14 C15	D2 D3

Objective questions exam	Two multiple-choice tests with questions on theoretical topics will be scheduled throughout the term.	20	B3 B4	C14 C15
Problem and/or exercise solving	Three tests which include problem solving and/or exercises on theoretical topics will be scheduled throughout the term.	30	B3 B4	C14 C15

Other comments on the Evaluation

The final mark will be expressed in numerical form ranging from 0 to 10.

The students will be offered two assessment systems: continuous assessment and exam-only assessment.

It is considered that the students who deliver the first assessable practice have chosen continuous assessment.

By default, if a student does not deliver the first assessable practice, it is assumed that it is in a exam-only assessment.

The students that opt for the exam-only assessment will not be assessed in any of the tasks of continuous assessment.

All the tasks must be delivered in the date specified by the professor, otherwise they will not be assessed.

In case of detection of plagiarism in any of the tasks (theoretical exam, laboratory practices or autonomous projects) the final qualificationwill be fail (0) and the fact will be communicated to the Head of the faculty for further actions.

The subject is composed of a theoretical part and a laboratory part. Each of them represents 50 % of the total mark of the subject.

CONTINUOUS ASSESSMENT (first call)

Laboratory class attendance is compulsory if the student has chosen continuous assessment.

The students who have chosen continuous assessment can only miss 1 laboratory session without justification, as a maximum.

The students that do not attend a session with justification, will receive a 0 mark in that session, but they will still be considered to be in continuous assessment.

Nevertheless, if a student misses more than 3 sessions, even with justification, they will have to realise an individual additional task to be allowed to remain in continuous assessment.

If the number of students in any laboratory group is sufficiently small, the students will carry out the practices and projects individually. Otherwise, students will perform these tasks in groups of 2. In the latter case, the two students will receive the same mark.

Theoretical class attendance is considered crucial to achieve success in continuous assessment, as the experience shows that it has a strong influence on the rate of success in the continuous assessment.

All the tasks have to be delivered on the date specified by the professor, otherwise they will not be assessed.

None of the tasks can be done on a different date that the one set up by the professor.

If any of the previous conditions is not met, the student that was in continuous assessment will lose the right to it and will automatically fail.

The total mark will be the sum of the marks obtained in the different tasks of the subject.

To pass the subject, it is necessary that:

· The global mark of the theory (TM) is greater or equal than 4 over 10.

· The global mark of the laboratory (LM) is greater or equal than 5 over 10.

· The global mark of the subject (FM) is greater or equal than 5 over 10.

The theory mark is calculated as follows:

TM = 0.20 * TE1 + 0.20 * TE2 + 0.20 * EX1 + 0.20 * EX2 + 0.20 * EX3

being:

TE1 and TE2: Mark of test exams.

EX1, EX2 and EX3: Mark of problems and/or exercises.

The laboratory mark is calculated as follows:

LM = 0.10 * LP1 + 0.10 * LP3 + 0.20 * LP4 + 0.30 * LAP1 + 0.30 * LAP2

being:

LP1, LP3 and LP4 = Mark of laboratory practices.

LAP1 = Laboratory Autonomous Project that consists of the design of a complex peripheral.

LAP2 = Laboratory Autonomous Project that consists of the design of a medium-complexity embedded system.

In case a student passes all the minimum marks, the final mark (FM) will be:

FM = 0.50 * TM + 0.50 * LM

In case a student does not reach any of the minimum marks (global theory mark < 4 or global laboratory mark < 5), the final mark (FM) will be:

FM = minimum [4.5; (0.50 * TM + 0.50 * LM)]

being:

TM = Global theory mark.

LM = Global laboratory mark.

The students that pass the course by means of continuous assessment will not be allowed to repeat any tasks (theory, laboratory) in the exam-only assessment in order to improve the mark.

If the students who are following continuous assessment deliver all the tasks, the mark of the part of the subject (theory, laboratory) in which they have obtained the minimum demanded will be preserved, only until the second call of the same academic course.

EXAM-ONLY ASSESSMENT(first or second call) AND END-OF-PROGRAM CALL

The students that opt for the exam-only assessment (whether it is the first or the second call) or for the end-of-program call will have to do a theoretical exam and a laboratory exam individually.

To be allowed to do the laboratory exam, it is necessary to request it previously on the dates that will be communicated to the students through the FaiTIC website.

The total mark will be the sum of the marks obtained in the different tasks of the subject.

To pass the subject, it is necessary that:

· The mark of the theoretical exam is greater or equal to 4 over 10.

· The mark of the laboratory exam is greater or equal to 5 over 10.

· The global mark of the subject is greater or equal to 5 over 10.

In case a student passes all the different tasks, the final mark (FM) will be the weighted sum of the marks of each exam:

FM = 0.50 * TE + 0.50 * LE

In case a student does not pass one of the exams (theoretical exam < 4 or laboratory exam < 5), the final mark (FM) will be:

FM = minimum [4.5; (0.50 * TE + 0.50 * LE)]

being:

TE = Theoretical Exam.

LE = Laboratory Exam.

Theoretical exam

The theoretical exam will include test questions and practical problems on the topics of all the theoretical lessons. The students will have to answer all the exam questions correctly to obtain the maximum mark.

This exam will be held on the date and place that the faculty will determine.

Laboratory exam

The exam will consist of the design of circuits in VHDL and programs in assembler for the microprocessor used in the subject. These circuits and programs may be part of a complex peripheral or an embedded system and they will have a similar complexity to the ones designed in the laboratory practices and the autonomous laboratory projects during the continuous assessment.

The students will have to perform the simulations and tests described in the exam in the assigned time.

The teacher may request that the students show them the operation of each of the circuits and programs.

All the sections have to work perfectly to obtain the maximum mark.

The addition of additional functionality to the minimum required will be taken into account.

It is compulsory to deliver the files indicated in the exam.

If this condition is not fulfilled, the corresponding sections will not be assessed.

The correct operation and the correct application of the theoretical concepts to the circuits and programs realised during the exam will be assessed, according to the same assessment criteria for the laboratory practices and the autonomous projects during the continuous assessment.

Sources of information

Basic Bibliography

POZA GONZÁLEZ, F., ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño de sistemas empotrados de 8 bits en FPGAs con Xilinx ISE y Picoblaze**, Vision libros, 2012

Chu, Pong P., **FPGA prototyping by VHDL examples**, John Wiley & Sons, Inc., 2008

Complementary Bibliography

ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño Digital con FPGAs**, Vision libros, 2013

ÁLVAREZ RUIZ DE OJEDA, L.J.,, **Diseño Digital con Lógica Programable**, Editorial Tórculo, 2004

ÁLVAREZ RUIZ DE OJEDA, L. Jacobo, MANDADO PÉREZ, E., VALDÉS PEÑA, M.D., **Dispositivos Lógicos Programables y sus aplicaciones**, Editorial Thomson-Paraninfo, 2002

PÉREZ LÓPEZ, S.A., SOTO CAMPOS, E., FERNÁNDEZ GÓMEZ, S., **Diseño de sistemas digitales con VHDL**, Thomson-Paraninfo, 2002

Ken Chapman, **PicoBlaze 8-bit Embedded Microcontroller User Guide for Spartan-3, Spartan-6, Virtex-5, and Virtex-6 FPGAs (UG129)**, Xilinx, 2010

Ken Chapman, **KCPSM3, 8-bit Microcontroller for Spartan-3, Virtex-2 and Virtex-2 Pro (KCPSM3_Manual)**, Xilinx, 2003

Recommendations

Subjects that continue the syllabus

Design and synthesis of digital systems/V05G300V01923

Subjects that are recommended to be taken simultaneously

Electronic Systems for Signal Processing/V05G301V01312

Subjects that it is recommended to have taken before

Programming I/V05G301V01105
Digital electronics/V05G301V01203
Physics: Fundamentals of electronics/V05G301V01201

Other comments

The students will have previously followed the subject Digital Electronics. It gives the necessary knowledge to understand the topics of this course. It is not necessary to have passed it.

Besides, it is recommended that the students have previously followed the subject Physical: Foundations of Electronics and Programming I. They give the necessary knowledge to understand some topics of this course.

Contingency plan

Description

In case of having to teach partly or entirely online because of health and safety recommendations, the same teaching methodologies and assessment methods will be maintained.