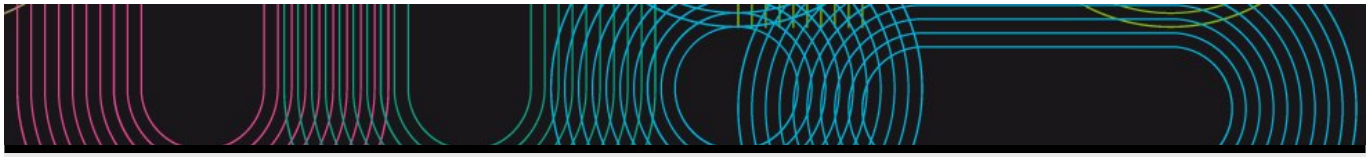

IDENTIFYING DATA				
Programmable Electronic Circuits				
Subject	Programmable Electronic Circuits			
Code	V05G300V01502			
Study programme	Degree in Telecommunications Technologies Engineering			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Mandatory	3rd	1st
Teaching language	Spanish Galician			
Department	Electronics Technology			
Coordinator	Álvarez Ruiz de Ojeda, Luís Jacobo			
Lecturers	Álvarez Ruiz de Ojeda, Luís Jacobo Poza González, Francisco Valdés Peña, María Dolores			
E-mail	jalvarez@uvigo.es			
Web	http://www.faitic.uvigo.es/			
General description	The main learning goals of this course are: Architecture of microprocessors, microcontrollers and configurable devices. Design methods and tools to acquire the necessary skills to design systems based on these devices.			

Competencies	
Code	
B3	CG3: The knowledge of basic subjects and technologies that enables the student to learn new methods and technologies, as well as to give him great versatility to confront and adapt to new situations
B4	CG4: The ability to solve problems with initiative, to make creative decisions and to communicate and transmit knowledge and skills, understanding the ethical and professional responsibility of the Technical Telecommunication Engineer activity.
B13	CG13 The ability to use software tools that support problem solving in engineering.
C7	CE7/T2: The ability to use communication and software applications (ofimatics, databases, advanced calculus, project management, visualization, etc.) to support the development and operation of Electronics and Telecommunication networks, services and applications.
C8	CE8/T3: The ability to use software tools for bibliographical resources search or information related with electronics and telecommunications.
C14	CE14/T9: The ability to analyze and design combinatory and sequential, synchronous and asynchronous circuits and the usage of integrated circuits and microprocessors.
C15	CE15/T10: The knowledge and application of the fundamentals of description languages for hardware devices.
D2	CT2 Understanding Engineering within a framework of sustainable development.
D3	CT3 Awareness of the need for long-life training and continuous quality improvement, showing a flexible, open and ethical attitude toward different opinions and situations, particularly on non-discrimination based on sex, race or religion, as well as respect for fundamental rights, accessibility, etc.

Learning outcomes		
Expected results from this subject		Training and Learning Results
To understand the basic architecture of microprocessors, microcontrollers and configurable devices (FPGAs).	B3	C14 C15
To know the methods and techniques of design of integrated hardware/software systems (System on Chip □ SoC).	B3	C14 C15
To know the hardware and software tools for the design of systems based in programmable devices.	B13	C14 C15
To acquire the skills to use the design tools for the design of digital systems.		C14 C15

Ability to design simple integrated systems (System on Chip □ SoC) applied to the telecommunications fields.	B3 B4 B13	C7 C8 C14 C15	D2 D3

Contents	
Topic	
LESSON 1 THEORY (1 h.). INTRODUCTION TO FPGAs.	1.1.- Introduction. 1.2.- Definition of FPGA. FPGA classification. 1.3.- FPGA architectures. 1.3.1.- Logical resources. 1.3.1.1.- Configurable Logic Blocks. 1.3.1.2.- Internal Logic Blocks. 1.3.1.3.- Input/Output Blocks. 1.3.1.4.- Embedded circuits. Memories. PLL digital circuits. Arithmetical circuits. Multipliers. DSP blocks. Serial transceivers. 1.3.2.- Interconnection resources. 1.3.2.1.- Interconnection lines. 1.3.2.2.- Configurable connection points. 1.3.3.- Examples of commercial FPGAs. 1.4.- FPGA technologies. 1.4.1.- FPGA manufacturing technologies (LVTTL, LVCMOS, etc.). 1.4.2.- FPGA configuration technologies. 1.4.2.1.- Static RAM technology (SRAM). 1.4.2.2.- Antifuse technology. 1.4.2.3.- Non-volatile memory technology (EEPROM). 1.4.3.- FPGA configuration. Methods. External programmer. In System Programmable (ISP). 1.5.- General characteristic of the FPGAs. 1.6.- Advantages of the FPGAs. 1.7.- Stages of the design of digital systems with FPGAs. 1.7.1.- Design implementation with FPGAs. 1.8.- FPGA CAD tools. 1.9.- FPGA applications. 1.10.- FPGAs versus other circuits. Comparative analysis.
LESSON 2 THEORY (1 h.). XILINX ARTIX 7 FPGA FAMILY. ARCHITECTURE.	2.1.- Introduction. 2.2.- Xilinx Artix 7 family architecture. 2.2.1.- Logical resources. CLBs. □Slices□. RAM-based shift registers. 2.2.2.- Internal memories. Distributed memory. Embedded memory. 2.2.3.- Clock circuits. 2.2.4.- DSP circuits. 2.2.5.- Input / Output technologies. 2.3.- Synthesis guidelines.
LESSON 3 THEORY (2 h.). INTRODUCTION TO MICROCONTROLLERS.	3.1.- Introduction. Definition of microcontroller. 3.2.- Internal architecture. Harvard. Von Neumann. 3.2.1.- Control Unit. 3.2.2.- ALU. 3.2.3.- Instruction set. RISC. CISC. 3.3.- External architecture. 3.3.1.- Access to memory. Program memory. Data memory. 3.3.2.- Access to peripherals. Input / Output ports. 3.3.3.- Interrupt control. 3.4.- Integrated peripherals. 3.4.1.- Timers. 3.4.2.- Serial communication. UART RS232. SPI. I2C. 3.4.3.- A/D and D/A converters. 3.5.- Examples of commercial microcontrollers. 3.6.- Microcontroller applications. 3.7.- Tools for programming and verification.
LESSON 4 THEORY (2 h.). XILINX PICOBLAZE MICROPROCESSOR (I).	4.1.- Introduction. 4.2.- Versions of the Xilinx Picoblaze microprocessor. 4.3.- Internal architecture of the Picoblaze microprocessor. 4.4.- Instruction set of the Picoblaze microprocessor.
LESSON 5 THEORY (1 h.). SOFTWARE DEVELOPMENT FOR XILINX PICOBLAZE MICROPROCESSOR.	5.1.- Introduction. 5.2.- Syntax of an assembler program for the Picoblaze microprocessor. 5.3.- Program development with pBlazeIDE environment for Picoblaze .

LESSON 6 THEORY (3 h.). XILINX PICOBLAZE MICROPROCESSOR (II).	6.1.- Introduction. 6.2.- External architecture. 6.2.1.- Input / Output instructions. 6.2.2.- Connection of input peripherals. 6.2.3.- Connection of output peripherals. 6.2.4.- Initial state. 6.2.5.- External interrupts. 6.3.- Design of peripherals for the Picoblaze microprocessor.
LESSON 7 THEORY (1 h.). INTRODUCTION TO SYSTEMS ON CHIP (SOC).	7.1.- Introduction to digital design methods. 7.1.1.- Software method. 7.1.2.- Hardware method. 7.2.- Systems On Chip (SOC). 7.3.- Systems On a Programmable Chip (PSOC). Microprocessors embedded in FPGAs. 7.3.1.- Hardware Microprocessors. 7.3.2.- Software Microprocessors. 7.4.- Embedded microprocessor applications.
LESSON 8 THEORY (4 h.). HARDWARE / SOFTWARE CODESIGN.	8.1.- Introduction. 8.2.- Software design. 8.3.- Hardware design. 8.4.- Stages of hardware / software codesign. 8.5.- Hardware / software partition. 8.6.- Examples hardware / software codesign. 8.7.- Peripheral design. How to split functions between hardware and software.
LESSON 9 THEORY (6 h.). DESIGN OF COMPLEX SYSTEMS.	9.1.- Introduction. 9.2.- Previous analysis of the most suitable solution. 9.3.- Application specific peripherals. Design methods. 9.3.1.- Practical examples.
LESSON 10 THEORY (2 h.). INTRODUCTION TO CORRECT DESIGN METHODS.	10.1.- Introduction. 10.2.- Design of digital systems with FPGAs. 10.2.1.- Hierarchical design. 10.2.2.- Independent technology design. 10.2.3.- Timing design.
LESSON 11 THEORY (3 h.). SYNCHRONOUS DIGITAL SYSTEM DESIGN.	11.1.- Introduction. 11.2.- Synchronous design. 11.3.- Synchronous sequential systems. FPGA design tips. 11.4.- Synchronisation of input variables.
LESSON 1 LABORATORY (2 h.). STAGES OF DIGITAL SYSTEM DESIGN WITH FPGAs.	1.1.- Introduction. Xilinx Vivado tool flow diagram. 1.2.- VHDL description. 1.3.- Behavioural simulation. 1.4.- Synthesis. 1.5.- Implementation. 1.6.- Implementation options for Xilinx FPGA families. 1.7.- FPGA Editor. 1.8.- Timing simulation. 1.9.- Timing analysis report. 1.10.- Technology and configuration methods for Xilinx FPGAs. 1.11.- Development boards based on FPGAs of Xilinx. 1.12.- Configuration file (.BIT). 1.13.- FPGA programming. 1.14.- Digital system testing. Frequent problems. 1.15.- Examples.
LESSON 2 LABORATORY (2 h.). PERIPHERAL CIRCUIT DESIGN FOR THE PICOBLAZE MICROPROCESSOR.	2.1.- Introduction. 2.2.- Guidelines on synchronous design with VHDL. 2.3.- Basic register in VHDL. 2.4.- Data memory in VHDL. 2.5.- Timer in VHDL.
LESSON 3 LABORATORY (2 h.). PERIPHERALS INTERFACE CIRCUIT DESIGN FOR THE PICOBLAZE MICROPROCESSOR.	3.1.- Introduction. 3.2.- Input peripheral interface circuit in VHDL. 3.3.- Output peripheral interface circuit in VHDL. 3.4.- Interrupt storing circuit in VHDL.
LESSON 4 LABORATORY (2 h.). XILINX PICOBLAZE MICROPROCESSOR SOFTWARE TOOLS.	4.1.- Introduction. 4.2.- Program assembler and simulator in Mediatronix. Picoblaze IDE. 4.3.- Basic examples.

LESSON 5 LABORATORY (6 h.). DESIGN OF DIGITAL SYSTEMS BASED ON THE PICOBLAZE MICROPROCESSOR.	5.1.- Introduction. 5.2.- Picoblaze microprocessor source files. 5.3.- Design stages for digital systems based on the Picoblaze microprocessor. 5.3.1.- Choosing the right Picoblaze microcontroller. 5.3.2.- Picoblaze program design. 5.3.3.- Picoblaze program simulation. 5.3.4.- Generation of the necessary VHDL files for the implementation of the Picoblaze Microprocessor in Xilinx Spartan 3E FPGA family. 5.3.5.- Peripheral circuit design for the Picoblaze microcontroller. Additional circuits needed. 5.3.6.- Simulation of the peripheral and additional circuits. 5.3.7.- Implementation of the complete digital system. 5.3.8.- Test of the complete digital system. 5.4.- Design of a basic example with use of interrupts, based on the Picoblaze microprocessor.
LESSON 6 LABORATORY (6 h.). PROJECTS. DESIGN OF PERIPHERALS FOR THE PICOBLAZE MICROPROCESSOR.	6.1.- Design and implementation of a medium-complexity peripheral for the Picoblaze 3 microprocessor, according to the instructions supplied by the teacher through FaiTIC website.
LESSON 7 LABORATORY (6 h.). PROJECTS. DESIGN OF AN EMBEDDED SYSTEM BASED ON THE PICOBLAZE MICROPROCESSOR.	7.1.- Design and implementation of a medium-complexity application example based on the Picoblaze 3 microprocessor, according to the instructions supplied by the teacher through FaiTIC website.

Planning

	Class hours	Hours outside the classroom	Total hours
Introductory activities	2	2	4
Lecturing	12	16	28
Problem solving	12	19	31
Laboratory practices	14	20	34
Supervised work	12	24	36
Essay questions exam	4	13	17

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies

	Description
Introductory activities	Introduction to the subject key topics both theoretical and practical. Through this methodology the outcome CG3 is developed.
Lecturing	Conventional lectures. Through this methodology the outcome CG3 is developed.
Problem solving	These sessions will include the realisation of exercises and works by part of the professor and of the students. Through this methodology the outcomes CG3, CG4, CE8/T3, CE14/T9 and CE15/T10 are developed.
Laboratory practices	Guided practices will be set out in these sessions , as well as the realisation of circuits and programs. Through this methodology the outcomes CG3, CG4, CG13, CE7/TE2, CE8/T3, CE14/T9, CE15/T10, CT2 and CT3 are developed.
Supervised work	The students will have to develop a laboratory project which consists of designing circuits and programs. This project is related to the laboratory lesson 6. Through this methodology the outcomes CG3, CG4, CG13, CE7/TE2, CE8/T3, CE14/T9, CE15/T10, CT2 and CT3 are developed.

Personalized attention

Methodologies	Description
Laboratory practices	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.
Supervised work	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.

Assessment

	Description	Qualification	Training and Learning Results		
Laboratory practices	Design of digital circuits in VHDL and assembler programs. It will be necessary to deliver the design source files and show the teacher in the laboratory the operation of each one of the circuits and programs. The assessment will be based on the operation of the circuits and programs developed in the practical sessions corresponding to the laboratory lesson 5, according to the published criteria. Through this methodology the outcomes CG3, CG4, CG13, CE7/TE2, CE8/T3, CE14/T9, CE15/T10, CT2 and CT3 are assessed.	10	B3 B4 B13	C7 C8 C14 C15	D2 D3
Supervised work	Autonomous Project. The students will have to develop two autonomous projects. The first project will consist of designing a complex peripheral. The peripheral must be composed of a control unit and an ALU and must be designed following the method analysed in the theoretical lesson 9. The content corresponds with laboratory lesson 6. The second project will consist of designing a medium-complexity embedded digital system. The embedded system must be composed of a microprocessor and its peripherals, as well as the auxiliary circuits needed to work correctly. It will also be necessary to develop a program for the microprocessor in assembler language. The content corresponds with laboratory lesson 7. In both projects the assessment will be based on the correct operation of the circuits and programs developed during the laboratory sessions assigned to the abovementioned lessons, as well as on the correct application of the theoretical concepts to the job done, according to the published criteria. It will be necessary to show every circuit and program to the teacher in the laboratory. Through this methodology the outcomes CG3, CG4, CG13, CE7/TE2, CE8/T3, CE14/T9, CE15/T10, CT2 and CT3 are assessed.	40	B3 B4 B13	C7 C8 C14 C15	D2 D3
Essay questions exam	This exam will include two types of questions: 1) Multiple choice questions about the theoretical topics of the subjects. 2) Design problems about circuits and programs, explaining the work done Through this methodology the outcomes CG3, CE14/T9 and CE15/T10 are assessed.	50	B3 B4	C14 C15	

Other comments on the Evaluation

The final mark will be expressed in numerical form ranging from 0 to 10.

The students will be offered two assessment systems: continuous assessment and single assessment.

The students must choose at the beginning of the term between continuous assessment or single assessment.

The students that opt for the single assessment will not be evaluated in any of the tasks of continuous assessment.

All the tasks must be delivered in the date specified by the professor, otherwise they will not be assessed.

In case of detection of plagiarism in any one of the tasks (theoretical exam or laboratory practices and autonomous projects) the final qualification will be fail (0) and the fact will be communicated to the Head of the faculty for further actions.

The subject is composed of a theoretical part and a laboratory part. Each one of them represents 50 % of the total mark of the subject.

The theoretical part consists of a final examination. This final examination will be the same for all the students, regardless of the type of assessment they have opted for.

The exam will be on the date of the final exam of the semester, which the faculty will determine.

CONTINUOUS ASSESSMENT (first opportunity):

Laboratory class attendance is compulsory if the student has chosen continuous assessment.

The students who have chosen continuous assessment can only miss 1 laboratory session without justification, as a maximum.

The students that do not attend any sessions with justification, will receive a 0 mark 0 in those sessions, but they will still be considered in continuous assessment.

Nevertheless, if a student misses more than 3 sessions, even with justification, they will have to realise an individual additional task to be allowed to remain in continuous assessment.

The students will develop the laboratory practices and the laboratory projects in groups of two students during the continuous assessment, whenever possible. Both students will be given the same mark if they have attended the laboratory.

Theoretical class attendance is considered crucial to achieve success in continuous assessment,as the experience shows that it has a strong influence on the rate of success in the continuous assessment.

All the tasks have to be delivered on the date specified by the professor, otherwise they will not be assessed. . It is also compulsory to sit the theoretical exam in thecontinuous assessment.

None of the tasks can be done on a different date that the one set up by the professor.

If any of the previous conditions is not met, the student that was in continuous assessment will lose the right to it and will automatically fail.

The total mark will be the sum of the marks obtained in the different tasks of the subject.

To pass the subject, it is necessary that:

· The mark of the theoretical exam is greater or equal to 4 over 10.

· The global mark of the laboratory tasks is greater or equal to 5 over 10.

· The global mark of the subject is greater or equal to 5 over 10.

In case the students pass all the different tasks, the final mark (FM) will be the weighted sum of the marks of each part of the subject:

NF = 0.50 * TE + 0.10* LP + 0.20 * AP1 + 0.20 * AP2

In case the students do not pass some of the tasks of the subject (theoretical exam < 4 or global laboratory mark < 5), the final qualification (NF) will be:

NF = minimum [4.5; (0.50 * TE + 0.10 * LP + 0.20 * AP1 + 0.20 * AP2)]

Being:

TE = Theoretical Exam

LP = Mark of the guided laboratory practices corresponding to lesson 5.

AP1 = Laboratory Autonomous Project that consists of the design of a complex peripheral.

AP2 = Laboratory Autonomous Project that consists of the design of a medium-complexity embedded system.

The students that pass the course by means of continuous assessment will not be allowed to repeat any tasks in the single assessment in order to improve the mark.

If the students who are following continuous assessment deliver all the tasks and sit the theoretical exam do not pass the subject, the mark of the part of the subject (theory,laboratory) in which they have obtained the minimum demanded will be preserved, only until the extraordinary assessment of July of the same academic course.

SINGLE ASSESSMENT (first or second opportunity) AND EXTRAORDINARY CALL:

The students that opt for the single assessment (whether it is the first or the second opportunity) or for the extraordinary call will have to do a theoretical exam and a laboratory exam individually.

To be allowed to do the laboratory exam, it is necessary to request it previously on the dates that will be communicated to

the students through the FaiTIC website.

The total mark will be the sum of the marks obtained in the different tasks of the subject.

To pass the subject, it is necessary that:

· The mark of the theoretical exam is greater or equal to 4 over 10.

· The mark of the laboratory exam is greater or equal to 5 over 10.

· The global mark of the subject is greater or equal to 5 over 10.

In case the students pass all the different tasks, the final mark (FM) will be the weighted sum of the marks of each part of the subject:

NF = 0.50 * TE +0.50 * LE

In case the students do not pass some of the tasks of the subject (theoretical exam < 4 or laboratory exam < 5), the final qualification (NF) will be:

NF = minimum [4.5; (0.50 * TE + 0.50 * LE)]

Being:

TE = Theoretical Exam.

LE = Laboratory Exam.

Theoretical exams.

The theoretical exam will include practical problems and test questions on the topics of all the theoretical lessons. The students will have to answer all the exam questions correctly to obtain the maximum mark.

This exam will be held at the place and on the date that the faculty will determine.

Guided laboratory practices (only for continuous assessment).

Only the circuits and programs developed in the laboratory sessions which correspond to the laboratory lesson 5 will be evaluated.

Autonomous laboratory project (only for continuous assessment).

Assignment1. Complex peripheral. Design of a peripheral for the microprocessor used in the subject. The peripheral has to be composed of a control unit and an ALU, according to the method studied in the theoretical lesson 9 of the subject.

Assignment2. Embedded System. Design of an embedded system based on the microprocessor studied in the theory of the subject. This embedded system has to include the complex peripheral design in assignment 1.

The assessment criteria for both the laboratory practices (laboratory lesson 5) and the two laboratory projects are the following.

- All the sections have to work perfectly to obtain the maximum mark.

- The addition of additional functionality to the minimum required will be taken into account.

- It is compulsory to show the operation of each section in the practice session indicated by the professor.

- It is compulsory to deliver the files indicated in the practice before the deadline indicated by the professor.

If these conditions are not fulfilled, the corresponding sections will not be assessed.

Laboratory exam (only for single assessment).

The exam will consist of the design of circuits in VHDL and programs in assembler for the microprocessor used in the subject. These circuits and programs may be part of a complex peripheral or an embedded system and they will have a similar complexity to the ones designed in the laboratory practices and the autonomous laboratory projects of the continuous assessment.

The students will have to realise the simulations and board test described in the exam in the assigned time.

It is compulsory to show the operation of each section to the professor in the laboratory the day of the exam.

All the sections have to work perfectly to obtain the maximum mark.

The addition of additional functionality to the minimum required will be taken into account.

It is compulsory to deliver the files indicated in the exam.

If these conditions are not fulfilled, the corresponding sections will not be assessed.

The correct operation and the correct application of the theoretical concepts to the circuits and programs realised during the exam will be evaluated, according to the same assessment criteria for the laboratory practices and the autonomous projects during the continuous assessment.

Sources of information

Basic Bibliography

ÁLVAREZ RUIZ DE OJEDA, L.J.,, **Diseño Digital con Lógica Programable**, Editorial Tórculo, 2004

POZA GONZÁLEZ, F., ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño de sistemas empotrados de 8 bits en FPGAs con Xilinx ISE y Picoblaze**, Vision libros, 2012

Complementary Bibliography

ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño Digital con FPGAs**, Vision libros, 2013

ÁLVAREZ RUIZ DE OJEDA, L. Jacobo, MANDADO PÉREZ, E., VALDÉS PEÑA, M.D., **Dispositivos Lógicos Programables y sus aplicaciones**, Editorial Thomson-Paraninfo, 2002

PÉREZ LÓPEZ, S.A., SOTO CAMPOS, E., FERNÁNDEZ GÓMEZ, S., **Diseño de sistemas digitales con VHDL**, Thomson-Paraninfo, 2002

Ken Chapman, **PicoBlaze 8-bit Embedded Microcontroller User Guide for Spartan-3, Spartan-6, Virtex-5, and Virtex-6 FPGAs (UG129)**, Xilinx, 2010

Ken Chapman, **KCPSM3, 8-bit Microcontroller for Spartan-3, Virtex-2 and Virtex-2 Pro (KCPSM3_Manual)**, Xilinx, 2003

Recommendations

Subjects that continue the syllabus

Design and synthesis of digital systems/V05G300V01923

Subjects that it is recommended to have taken before

Programming I/V05G300V01205
Digital Electronics/V05G300V01402
Physics: Fundamentals of Electronics/V05G300V01305

Other comments

The students will have previously followed the subject Digital Electronics. It gives the necessary knowledge to understand the topics of this course. It is not necessary to have passed it.

Besides, it is recommended that the students have previously followed the subject Physical: Foundations of Electronics and Programming I. They give the necessary knowledge to understand some topics of this course.