



IDENTIFYING DATA

Advanced Digital Electronic Systems

Subject	Advanced Digital Electronic Systems			
Code	V05M145V01203			
Study programme	Telecommunication Engineering			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	5	Mandatory	1st	2nd
Teaching language	Spanish			
Department				
Coordinator	Moure Rodríguez, María José			
Lecturers	Moure Rodríguez, María José Valdés Peña, María Dolores			
E-mail	mjmoure@uvigo.es			
Web	http://fatic.uvigo.es			
General description	The objective of this course is to provide students with the ability to design complex or high frequency digital systems. Firstly, the electrical characteristics, power consumption, speed and fan-out of digital integrated circuits and the technologies of semiconductor memories are studied. Subsequently, the interface with external peripherals and the methodology for designing synchronous sequential systems are analyzed. Finally, the course focuses on the design of digital communications systems implemented using high density of integration programmable circuits. Meanwhile, throughout all contents, emphasis is placed in the VHDL description of high complexity digital systems.			

Competencies

Code	
A4	CB4 Students must communicate their conclusions, and the knowledge and reasons stating them-, to specialists and non-specialists in a clear and unambiguous way.
A5	CB5 Students must have learning skills to allow themselves to continue studying in largely self-directed or autonomous way
B4	CG4 Capacity for mathematical modeling, calculation and simulation in technological centers and engineering companies, particularly in research, development and innovation tasks in all areas related to Telecommunication Engineering and associated multidisciplinary fields.
B8	CG8 Ability to apply acquired knowledge and to solve problems in new or unfamiliar environments within broader and multidiscipline contexts, being able to integrate knowledge.
C10	CE10 Ability to design and manufacture integrated circuits.
C11	CE11 Knowledge of hardware description languages for high complexity circuits.
C12	CE12 Ability to use programmable logic devices, as well as to design advanced electronic systems, both analog and digital. The ability to design communications components such as routers, switches, hubs, transmitters and receivers in different bands.
C14	CE14 Ability to develop electronic instrumentation, as well as transducers, actuators and sensors.

Learning outcomes

Expected results from this subject	Training and Learning Results
The knowledge of the different technologies of integrated circuits manufacture.	C10
The ability to analyze and design advanced digital circuits.	B4 C12
The knowledge of different input/output technologies of digital circuits.	C14
The ability to design input/output interface circuits.	C10 C12 C14
The knowledge of the methodologies for the design of complex digital circuits.	A5 B8 C12

The ability to design communication components using programmable logic devices.	A4 B8 C11 C12
The ability to design complex digital electronic systems using hardware description languages.	C11

Contents

Topic	
Introduction to digital integrated circuits	CMOS technology: NMOS and PMOS technologies, CMOS gates, CMOS fabrication. HW design methodologies: custom, semicustom, cell-based, array-based, programmable logic devices (FPGAs). SW design methodologies: abstraction levels, design methods, design flow, IPs.
Advanced VHDL	VHDL description of complex digital systems: variables, arrays, records, generics, generate, function, procedure. VHDL coding of Finite State Machines. Advances synthesis: inference, primitives, IPs.
CMOS integrated circuits	Design Metrics: voltages, noise, fan-in, fan-out, delay, power. Power issues in FPGAs Input/Output: standard levels, package. Timing issues: set-up, hold, metastability, skew, jitter, clock distribution.
Sequential design	Synchronizers: asynchronous inputs, PLLs, DLLs Clocking resources in FPGAs. Sequential Design methods: Moore and Mealy Finite State Machines.
Semiconductor memories	Architecture of semiconductor memories: RAM, CAM, ROM, EEPROM, FLASH. Memory Interfacing: RAM, DRAM, EEPROM, FLASH interfacing. Memory in FPGAs: distributed, blocks, external memory, memory IPs.
Sampling and signal reconstruction	Analog-to-digital conversion (ADC). Sampling rate. Aliasing. Quantization error. Clock signal generation using FPGAs. Jitter error. Digital-to-analog conversion (DAC). Anti-alias and reconstruction filters.
Arithmetic in FPGAs	Numeric representations. Overflow. Techniques to mitigate overflow. Precision vs. hardware cost. Arithmetic operations. Low cost hardware implementations. Design arithmetic considerations for HDL coding.
Frequency synthesis for communication applications	Frequency synthesis using numerically controlled oscillators (NCOs). NCO architecture. Design parameters. Spurious Free Dynamic Range (SFDR) characterization. Design techniques. NCO implementation using FPGAs.
Retiming and pipeline techniques	Signal flow graphs (SFGs). Analysis of the critical path of digital systems. Analysis of the input to output latency. Retiming techniques to reduce propagation delay in digital systems: pipelining and time scaling. Applying retiming techniques to the design of digital filters. Hardware cost.
Series vs. parallel implementation issues	Applying the concepts to the implementation of digital filters using FPGAs. Design techniques: fully serial, fully parallel, serial-parallel. Hardware cost and timing issues. Applying the concepts to the implementation of digital filters using FPGAs.

Design and implementation of ADC/DAC interfaces, sensor interfaces, digital signal processing modules, communications blocks and memory interfaces.

Planning

	Class hours	Hours outside the classroom	Total hours
Master Session	18	20	38
Laboratory practises	14	10	24
Projects	5	30	35
Short answer tests	2	20	22
Practical tests, real task execution and / or simulated.	0	5	5
Jobs and projects	1	0	1

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies

	Description
Master Session	The professor explains the theoretical contents of the course, encouraging critical discussion and the student involvement. Reading assignments for each session will be previously available via FaiTIC, and students are expected to come to the theoretical class having completed the assigned reading.
	Through master sessions the outcomes CB5, CE10, CE11, CE12 and CE14 are developed.
Laboratory practises	During laboratory sessions students apply the design methods described in the master sessions. All the sessions are guided and supervised by the professor. The in-person sessions are developed in a laboratory with skilled equipment.
	Through laboratory practises the outcomes CG4, CE10, CE11, CE12 and CE14 are developed.
Projects	This activity focuses on applying the techniques described in the lecture classes and the skills developed at laboratory to a project implementation. The in-person sessions are developed in a laboratory with skilled equipment. Students should obtain well founded solutions, choosing appropriate methods and devices. These projects are planned and tutored in small size groups.
	Through master sessions the outcomes CB4, CB5, CG4, CG8, CE10, CE11, CE12 and CE14 are developed.

Personalized attention

Methodologies	Description
Master Session	Students have the opportunity to solve doubts in personalized attention sessions. The appointment with the corresponding professor should be required and agreed by e-mail, preferably in the hours which are published in the faculty website.
Laboratory practises	Students have the opportunity to solve doubts in personalized attention sessions. The appointment with the corresponding professor should be required and agreed by e-mail, preferably in the hours which are published in the faculty website.
Tests	Description
Jobs and projects	Each group of students developing a project will attend periodic follow-up meetings.

Assessment

	Description	Qualification	Training and Learning Results
Short answer tests	An objective evaluation will be realized at the end of the term. This exam assesses all of the contents taught in the theoretical classes.	30	C10 C11 C12 C14
Practical tests, real task execution and / or simulated.	This evaluation are realized during the practical sessions. The assistance to the laboratory practices is mandatory and the student should complete at least 4 of the 5 sessions. The implementation of the circuits described in the practice guidelines and the reports submitted at the end on each session will deserve the 20% of the final qualification.	20	B4 C10 B8 C11 C12 C14

Jobs and projects	During the first weeks of the term a job will be assigned to each student individually. This task will be related to any topics of the course and deserves the 20% of the final qualification. Besides at the end of the term the students should also present a tutored project which deserves the 30% of the final qualification. The progress of this job will be supervised from continuous assessment but the final work should be oral presented by the authors.	50	A4 B4 C10 A5 B8 C11 C12 C14
-------------------	--	----	--------------------------------------

Other comments on the Evaluation

1. Continuous assessment

The course can be passed with full marks from continuous assessment, with no need to sit the final exam. Students who assist to more than 2 laboratory sessions are graded using continuous assessment.

The weighting and content of each continuous assessment part are as follows:

1.1 Test (NExam):

- It covers all of the contents taught in the theoretical classes and includes short exercises or problems.
- The date of this test will be the same of the final exam.
- The student pass this part if he/she gets a mark greater than or equal to 5 over 10.

1.2 Laboratory practices (NPrac):

- The student should complete 4 of the 5 sessions in order to pass this part.
- The student should correctly implement the circuits described in the guidelines of the practice and submit a report corresponding to each laboratory session. The qualification of each practice depends on these achievements.
- It can be developed individually or by groups of 2 students. In this last case and if both attend the practice, the qualification is the same for the 2 students.

1.3 Job (NTask):

- This task will be assigned to each student individually.
- The student should present a written report of this task.

1.4 Project (NPro):

- It should be oral presented by each of the authors.
- It should be carried out by collaborative groups of 2 or more students. The 60% of the final mark (NPro) is obtained from the individual tasks assigned to each student, the 20% from the global tasks of the group, the 10% from the oral presentation of each student and the 10% from the report of the project.
- In case of plagiarism or abandonment of a member of a work group is detected, his/her score will be 'fail' (0) and will not compute for the score of the rest of the group.
- The student will pass this part if he/she gets a mark greater than or equal to 5 over 10.

1.5 Final qualification of continuous assessment (Final_ca)

The final qualification (Final_ca) of continuous assessment is obtained as follows:

Final_ca: = (NExam*0.3 + NPrac*0.2 + NTask*0.2 + NPro*0.3) if NExam and Npro are greater than or equal to 5;

Final_ca = min [(NExam*0.3 + NPrac*0.2 + NTask*0.2 + NPro*0.3), 4] in other case;

The student who fails one or more of the parts of continuous assessment has another opportunity to pass the following parts in the final exam:

- He/she can improve his/her assigned job and this mark replaces the previous one (NTask).
- He/she can repeat the theoretical examination and this mark replaces the previous one (NExam).
- He/she can complete and present his/her project and this mark replaces the previous one (NPro).

2. Final exam and qualification

There is a final exam at the end of the term and in July.

- In the final exam, all content is evaluated. It usually consists of several questions and problems and lasts 2 hours. The pass mark for this exam is 4 out of 10 and deserves 50% of the final qualification (NExam).
- The students must present the results and reports of the same practices developed in continuous assessment. This practices represent 20% of the final qualification (NPrac).
- In order to pass the subject the students should present an individual project with the same objectives and complexity of the project developed in continuous assessment. This project deserves 30% of the final qualification (NPro) and it is necessary to obtain a mark greater o equal to 5 out of 10 in order to pass the course.

Final_ex = (NExam*0.5 + NPrac*0.2 + NPro*0.3) if NExam and Npro are greater than or equal to 5;

Final_ex = min [(NExam*0.5 + NPrac*0.2 + NPro*0.3), 4] in other case;

3. Other comments

- The student can use the Spanish, English or Galician for the reports, works, exams or presentations.
- The grades obtained from the continuous assessment and final exams are only valid for the current academic year.
- The use of books, notes or electronic devices such as phones or computers is not permitted in any test or exam. Mobile phones must be turned off and be out of reach of the student.
- In the case that plagiarism is detected in any of the reports/tasks/exams done/taken, the final score for the subject will be 'fail' (0) and the teachers will inform the School authorities so that they take the actions that they consider appropriate.

Sources of information

Basic Bibliography

Complementary Bibliography

Weste N., Harris D., **CMOS VLSI Design. A circuits and systems perspective**, 4, 2011

Roth C.H., John L.K., **Digital systems design using VHDL**, 3, 2008

Sharma A.K., **Semiconductor memories : technology, testing, and reliability**, 1997

Kurinec S.K., Iniewski K., **Nanoscale Semiconductor Memories: Technology and Applications (Devices, Circuits, and Systems)**, 2013

Kleitz W., **Digital Electronics: A Practical Approach with VHDL**, 9, 2011

Comer D.J., **Digital logic and state machine design**, 3, 1995

Wakerly J.F., **Digital Design. Principles and Practices**, 4, 2007

Moure M.J., Valdés M.D.; **Apuntes y prácticas de SEDA**, 2017

Recommendations