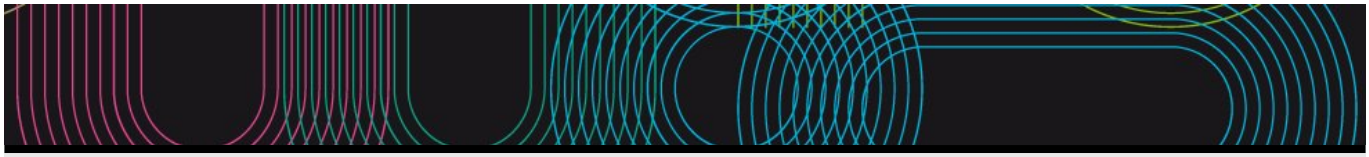

IDENTIFYING DATA				
Hardware/Software Design of Embedded Systems				
Subject	Hardware/Software Design of Embedded Systems			
Code	V05M145V01214			
Study programme	Telecommunication Engineering			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	5	Optional	1st	2nd
Teaching language	Galician English			
Department				
Coordinator	Poza González, Francisco			
Lecturers	Álvarez Ruiz de Ojeda, Luís Jacobo Poza González, Francisco			
E-mail	fpoza@uvigo.es			
Web	http://www.faitic.uvigo.es			
General description	The documentation of the subject will be in English. Half of lectures will be given in English, another half in galician. The main learning goals of this course are: □ To learn the codesign methods to design applications based on embedded microprocessors in FPGAs. □ To get to know the microprocessors that can be implemented in commercial FPGAs. □ To handle the necessary software tools for the development of embedded applications by means of FPGAs. □ To design application specific peripherals and their connection to the buses of the embedded microprocessors. □ To design real digital applications with embedded microprocessors in FPGAs.			

Competencies	
Code	
A5	CB5 Students must have learning skills to allow themselves to continue studying in largely self-directed or autonomous way
B1	CG1 Ability to project, calculate and design products, processes and facilities in telecommunication engineering areas.
B8	CG8 Ability to apply acquired knowledge and to solve problems in new or unfamiliar environments within broader and multidiscipline contexts, being able to integrate knowledge.
C11	CE11 Knowledge of hardware description languages for high complexity circuits.
C12	CE12 Ability to use programmable logic devices, as well as to design advanced electronic systems, both analog and digital. The ability to design communications components such as routers, switches, hubs, transmitters and receivers in different bands.

Learning outcomes	
Expected results from this subject	Training and Learning Results
To learn the codesign methods to design applications based on embedded microprocessors in FPGAs.	A5 C11 C12
To get to know the microprocessors that can be implemented in commercial FPGAs.	A5 C11 C12
To handle the necessary software tools for the development of embedded applications by means of FPGAs.	A5 C11 C12

To design application specific peripherals and their connection to the buses of the embedded microprocessors.	A5 B1 B8 C11 C12
To design real applications with embedded microprocessors in FPGAs.	A5 B1 B8 C11 C12

Contents	
Topic	
LESSON 1 THEORY. INTRODUCTION TO THE DESIGN OF EMBEDDED SYSTEMS. (1 h.)	1.1. Introduction. 1.2. Programmable Systems On Chip (PSOC). 1.3. Hardware/Software Codesign. Codesign phases. 1.4. Xilinx SOC Zynq family introduction. 1.5. Xilinx Vivado and SDK tools for codesign of embedded systems.
LESSON 2 THEORY. MICROPROCESSOR OF THE XILINX ZYNQ FAMILY SOCs. (0'5 h.)	2.1. ARM processor from Zynq SOC family (Zynq Processing Systems (PS)). 2.2. Processor peripherals from Zynq SOC family. 2.3. Clock, reset and processor debugging. 2.4. AXI interface.
LESSON 3 THEORY. FPGA OF THE XILINX ZYNQ FAMILY SOCs. (0'5 h.)	3.1. Introduction to 7 series Xilinx FPGAs. 3.1.1. Logic resources. 3.1.2. Input/output resources. 3.1.3. Memory and signal processing resources. 3.1.4. Analog to digital converter. 3.1.5. Clock resources.
LESSON 4 THEORY. CONNECTION OF PERIPHERAL CIRCUITS TO THE XILINX ARM MICROPROCESSOR. (1 h.)	4.1.- Introduction. 4.2.- Interface for basic peripherals. GPIO. 4.3.- Interface for advanced peripherals. IPIF. 4.4.- Interface for user coprocessors
LESSON 5 THEORY. SOFTWARE DEVELOPMENT FOR THE XILINX ARM MICROPROCESSOR. (1 h.)	5.1.- Introduction. 5.2.- Structure of the routines for handling of peripherals. 5.3.- Interrupt handle. 5.4.- Program debugging.
LESSON 6 THEORY. HARDWARE / SOFTWARE PARTITIONING. (1 h.)	6.1.- Introduction. 6.2.- Examples of hardware / software codesign. 6.3.- Distribution of tasks between hardware and software.
LESSON 7 THEORY. EMBEDDED SYSTEMS ANALISYS PROJECT. (5 h.)	7.1. Design of a software routine for the assigned function. 7.2. Design of a hardware peripheral (coprocessor) for the assigned function. 7.3. Profiling analysis from software routine and hardware peripheral. Comparison of results.
LESSON 1 LABORATORY. XILINX VIVADO ENVIRONMENT FOR THE DESIGN OF EMBEDDED SYSTEMS. (1.5 h.)	1.1. Introduction. 1.2. Xilinx Vivado environment. 1.3. Design of basic examples of embedded systems. 1.3.1. Addition of predefined peripherals (IP cores). 1.4. Implementation of the developed systems in Digilent evaluation boards.
LESSON 2 LABORATORY. DESIGN OF BASIC PERIPHERAL CIRCUITS. (2 h.)	2.1. Introduction. 2.2. Development of basic user peripherals. GPIO.
LESSON 3 LABORATORY. DESIGN OF ADVANCED PERIPHERAL CIRCUITS. (1.5 h.)	3.1. Introduction. 3.2. Development of advanced user peripherals (Custom IP).
LESSON 4 LABORATORY. XILINX SDK ENVIRONMENT FOR THE DESIGN OF EMBEDDED SYSTEMS SOFTWARE. (1 h.)	4.1. Introduction. 4.2. Xilinx Software Development Kit (SDK) environment. 4.3. Basic Design Examples.
LESSON 5 LABORATORY. SOFTWARE DEBUGGING OF EMBEDDED APPLICATIONS. (1 h.)	5.1. Introduction. 5.2. Software debugging of embedded systems by means of the GNU debugger from SDK.
LESSON 6 LABORATORY. HARDWARE VERIFICATION OF EMBEDDED APPLICATIONS. (1.5 h)	6.1. Introduction. 6.2. Embedded systems hardware verification using Vivado hardware analyzer.
LESSON 7 LABORATORY. EMBEDDED SYSTEMS PROFILING. (1.5 h)	7.1. Introduction. 7.2. Software profiler.

LESSON 8 LABORATORY. DESIGN PROJECT. DESIGN OF AN APPLICATION BASED IN XILINX 32-BIT MICROPROCESSORS. (10 h.: 5 h. type B + 5 h. type C)	8.1. Design and test of the assigned application.

Planning			
	Class hours	Hours outside the classroom	Total hours
Master Session	5	10	15
Troubleshooting and / or exercises	5	20	25
Laboratory practises	10	10	20
Tutored works	9	48	57
Presentations / exhibitions	1	7	8

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies	
	Description
Master Session	Conventional lectures. Through this methodology the outcomes CE11 and CE12 are developed.
Troubleshooting and / or exercises	Problem based learning (PBL): Problem solving. Design of synthesizable circuits in VHDL and software programs in C language. To solve them, the student has to previously develop certain outcomes. Through this methodology the outcomes CB5, CG1, CG8, CE11 and CE12 are developed.
Laboratory practises	VHDL design of digital circuits and circuit implementation in FPGAs and development of software programs in C language. Integration of both to build an embedded system in a FPGA. Through this methodology the outcomes CB5, CG8, CE11 and CE12 are developed.
Tutored works	Project based learning. The students must design an embedded system to solve a problem. In order to that, the students must plan, design and implement the necessary steps. Through this methodology the outcomes CB5, CG1, CG8, CE11 and CE12 are developed
Presentations / exhibitions	Exhibition of the results of the project developed. Through this methodology the outcomes CB5, CE11 and CE12 are developed.

Personalized attention	
Methodologies	**Description**
Master Session	In class, the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours, which will be published in the faculty website.
Laboratory practises	In class, the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours, which will be published in the faculty website.
Troubleshooting and / or exercises	In class, the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours, which will be published in the faculty website.
Tutored works	In class, the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours, which will be published in the faculty website.

Assessment				
	Description	Qualification	Training and Learning Results	
Troubleshooting and / or exercises	Problem Based Learning. Resolution of exercises and theoretical problems. They will be focused on the development of a software routine and a hardware peripheral for the assigned function to each student and compare the profiling of both in terms of execution time and used logical resources. The content corresponds to theoretical lesson 7. It will be necessary to show to the professor the operation of each one of the circuits and programs. The correct application of the theoretical concepts to the problems will be assessed, based on the published criteria. It will be necessary to deliver a short report explaining the work done.	25	A5	B1 C11 B8 C12

Laboratory practises	Design circuits and programs in the laboratory sessions corresponding to the laboratory lessons 1 to 5. It will be necessary to show to the professor the operation of each one of the circuits and programs. It will be necessary to deliver the design source files. The assessment will be based on the operation of the digital system and the correct application of the theoretical concepts, according to the published criteria.	25	A5	B8	C11 C12
Tutored works	Project Based Learning. Laboratory Project. Design of an embedded system. It will be necessary to deliver the files source of the work realized. It will be necessary to deliver the design source files. The assessment will be based on the operation of the embedded system and the correct application of the theoretical concepts, according to the published criteria.	40	A5	B1 B8	C11 C12
Presentations / exhibitions	It will be necessary to do an oral presentation of 15 minutes as a maximum about the work, according to the index supplied by the teacher.	10	A5		C11 C12

Other comments on the Evaluation

The total mark will be the sum of the marks obtained in the different tasks of the subject.

All the students, both those who follow the subject continuously and those who want to be assessed in the final exam at the end of the term or in the extraordinary exam in July, will have to do the tasks described in the previous section. The students that do not attend classes regularly will also have to do the same tasks as the students who attend classes.

The final mark will be expressed in numerical form ranging from 0 to 10, according to the valid regulation (Royal decree 1125/2003 of 5 September; BOE 18 September). Following the guidelines of the degree the students will be offered two assessment systems: continuous assessment and final assessment.

CONTINUOUS ASSESSMENT:

 The students are considered to have chosen the continuous assessment when they have done 2 laboratory practices and/or 2 reports of theoretical exercises.

 The students that have chosen continuous assessment, but do not pass the course, will have to do the final assessment in July.

 The students that pass the course by means of continuous assessment will not be allowed to repeat any task in the final assessment in order to improve the mark.

 The different tasks should be delivered in the date specified by the teacher, otherwise they will not be assessed for the continuous assessment.

 Preferably the students will develop the theoretical exercises, the laboratory practices and the laboratory projects individually. In case of doing them in groups of two students the mark will be the same for both.

 The students who want to be assessed in the continuous assessment can only miss two sessions as a maximum. If they miss more than 2 sessions, it will be compulsory to do an additional individual task or an examination.

FINAL ASSESSMENT:

 The students that opt for the final assessment will have to do all the theoretical and practical tasks and the project individually.

 The tasks for the final assessment have to be delivered before the official date of the examination set by the faculty.

COMMON FOR ALL THE STUDENTS

In case the students pass the theoretical exercises (TE), the laboratory practices (LAB) and the laboratory project (LP), that is, the mark of each part >= 5, the final mark (FM) will be the weighted sum of the marks of each part of the subject:

FM = 0'25 * TE + 0'25 * LAB + 0'40 * LP + 0'10 * OP

In case the students do not pass any of the three main parts of the subject, that is, the mark of any task < 5, the final mark (FM) will be:

FM = Minimum [4'5; (FM = 0'25 * TE + 0'25 * LAB + 0'40 * LP + 0'10 * OP)]

Where:

TE = Global mark of the theoretical exercises and problems.

LAB = Guided Laboratory Practices.

LP = Laboratory Project.

OP = Oral presentation.

ASSESSMENT CRITERIA.

1) Realization of guided laboratory practices.

It will evaluate the correct operation of the circuits and programs developed in the laboratory sessions. Each laboratory lesson will be marked from 0 to 10. Its influence in the total mark of the subject will be weighted in function of the number of hours assigned to each lesson.

That is, the mark of the practices corresponding to the laboratory lessons 1 to 5 will be obtained through the following formula:

LAB = (Lesson 1L + Lesson 2L + Lesson 3L + Lesson 4L + Lesson 5L) / 5

The total mark of the guided laboratory practices (LAB) will correspond to 25% of the total mark of the subject. It will be necessary to deliver the required source files. The assessment criteria refer only to the functionality of the circuits and programs developed, that is, the circuits and programs have to work perfectly to obtain the maximum mark.

2) Theoretical exercises and problems.

Each one of the theoretical exercises and problems proposed in the theoretical sessions will be marked from 0 to 10. Its influence in the total mark of the subject will be weighted in function of the number of exercises assigned.

The majority of the exercises will consist in the design of a peripheral for an embedded system and the approach to the design of a complete embedded system with its peripherals.

The assessment criteria are the following:

2.1) Suitable distribution of tasks between □hardware□ and □software".

2.2) Suitable organization of the □hardware□ and suitable structure of the C program.

2.3) Correct design (CORR).

Optimization of the VHDL description and the C programs. Synchronous design. Reusable design.

2.4) Functionality (FUNC).

If the exercise asks for it, the behavioral simulation and synthesis of the VHDL, as well as the simulation of the C programs have to work perfectly.

2.5) Documentation (DOC).

i. Design source files. Enough comments in the VHDL and C files to explain the sentences used.

It will be necessary to deliver the required source files. The total mark will be the sum of the marks of each one of the exercise reports divided by the number of reports:

TE = (Exercise 1 + □ + Exercise N) / N

3) Autonomous Laboratory Project.

This project consists in the design of an embedded system. The assessment criteria are the following:

3.1) Suitable distribution of tasks between □hardware□ and □software".

3.2) Suitable organization of the hardware system and suitable structure of the C program.

3.3) Correct design (CORR). System entirely synthesizable. Suitable hierarchy arrangement. Design totally synchronous. Technology independent design. Reusable design.

3.4) Analysis of the design and the implementation in FPGAs (ANA). Analysis of the FPGA logical resources used and their

justification. Analysis of the internal system delays. Analysis of the chosen implementation options. Optimal utilization of the FPGA logical resources. Achievement of an optimal processing speed. Verification with Chipscope.

3.5) Functionality (FUNC). Software Simulation. Software Debugging. Behavioral and Timing Simulation of the different hardware circuits. Simulation of the complete embedded system (hardware + software). Debugging of the complete embedded system (hardware + software). Board test of the complete embedded system (hardware + software). All the sections have to work perfectly to obtain the maximum mark.

6) Documentation of the design and the implementation with FPGAs (DOC).

3.6.1) Document.

i. Clear structure and order.

ii. Clear and sufficient explanations for the understanding of the work developed.

iii. Include suitable figures.

iv. Include important data.

3.6.2) Source design files.

i. Sufficient comments in the VHDL files for its understanding.

ii. Sufficient comments in the C files for its understanding.

For the Autonomous Laboratory Project (LP), it will be necessary to do an oral presentation.

3.7) Laboratory Project Oral Presentation.

The work developed during the laboratory project will be presented. The assessment criteria are the following:

i. Clear structure and presentation order.

ii. Clear explanations.

iii. Enough explanations to understand the project.

iv. Suitable figures.

v. Relevant data.

Sources of information

Basic Bibliography

ÁLVAREZ RUIZ DE OJEDA, L.J., POZA GONZÁLEZ, F., **Diseño de aplicaciones empotradas de 32 bits en FPGAs con Xilinx EDK 10.1 para Microblaze y Power-PC**, Vison Libros,

Complementary Bibliography

ÁLVAREZ RUIZ DE OJEDA, L.J., **Diseño Digital con FPGAs**, Vision Libros,

Recommendations

Subjects that are recommended to be taken simultaneously

Advanced Digital Electronic Systems/V05M145V01203