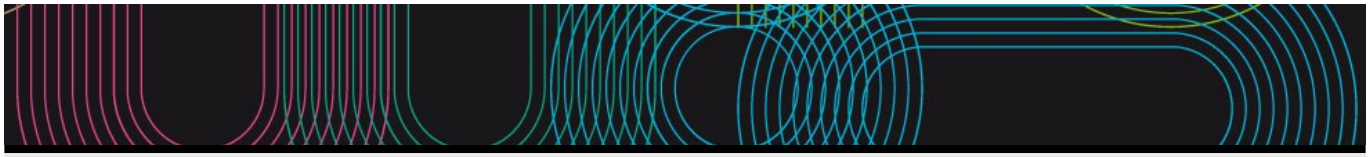

IDENTIFYING DATA				
Electronic Systems for Signal Processing				
Subject	Electronic Systems for Signal Processing			
Code	V05G300V01522			
Study programme	Degree in Telecommunications Technologies Engineering			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Optional	3rd	1st
Teaching language	Spanish			
Department				
Coordinator	Valdés Peña, María Dolores			
Lecturers	Valdés Peña, María Dolores			
E-mail	mvaldes@uvigo.es			
Web	http://www.faitic.uvigo.es			
General description	This course introduces the basic concepts of digital signal processing systems from the point of view of its hardware implementation. Emphasis is put on FPGAs-based solutions, using professional software design tools and hardware supports. The nature of the course is mainly practical. It enhances the development of collaborative projects whose ultimate goal is the design of electronic signal processing systems.			

Competencies	
Code	
B4	CG4: The ability to solve problems with initiative, to make creative decisions and to communicate and transmit knowledge and skills, understanding the ethical and professional responsibility of the Technical Telecommunication Engineer activity.
B6	CG6: The aptitude to manage mandatory specifications, procedures and laws.
B9	CG9: The ability to work in multidisciplinary groups in a Multilanguage environment and to communicate, in writing and orally, knowledge, procedures, results and ideas related with Telecommunications and Electronics.
B13	CG13 The ability to use software tools that support problem solving in engineering.
C39	(CE39/SE1): The ability to construct, exploit and manage the receiving, transporting, representation, processing, storage, manage and presentation multimedia information from the electronic systems point of view.
C45	(CE45/SE7): The ability to design interface, data capturing and storage devices, and terminals for services and telecommunication systems.
D2	CT2 Understanding Engineering within a framework of sustainable development.
D4	CT4 Encourage cooperative work, and skills like communication, organization, planning and acceptance of responsibility in a multilingual and multidisciplinary work environment, which promotes education for equality, peace and respect for fundamental rights.

Learning outcomes			
Expected results from this subject	Training and Learning Results		
Understand the fundamental design principles of the signal processing hardware systems.	B6 B13	C39 C45	
Ability to decide different design strategies depending on the application.	B4	C39 C45	D2
Ability to choice the most suitable hardware architecture for each application.	B4 B6	C39 C45	
Ability to design basic circuits for audio and image processing.	B4 B6 B9 B13	C39 C45	D4
Acquire skills in the use of design, simulation and implementation tools of signal processing systems.	B13	C39 C45	

Acquire skills to verify the proper operation of complex hardware systems.	B6 B13	C39 C45	
Acquire skills to combine different software tools and hardware platforms.	B13	C39 C45	
Ability to document hardware design projects.	B4 B9		D4

Contents	
Topic	
Theory: Theme 1. Introduction	- Basic architecture of electronic signal processing systems: signal conditioning, sampling, conversion, and reconstruction.
Theory: Theme 2. Types of signal processing	-Different hardware and software solutions: DSP and FPGAs. -Processing forms: Serial/Parallel, Hardware/Software. -Hardware cost of regular signal processing circuits. Logical resources used. Processing rate.
Theory: Theme 3. Arithmetic in DSP	-Data types. -Data modification: quantification and overflow. -Arithmetic operations and associated circuits. -Associated concepts: critical path, pipeline and latency.
Theory: Theme 4. Siignal conditioning and sampling	- Example of a real system for signal conditioning and sampling using a FPGA-based development board.
Theory: Theme 5. Design and Implementation of Digital Filters	- Implementation of digital filters in FPGA. - Analysis of full parallel and semi-parallel solutions: hardware costs, operation rates.
Theory: Theme 6. Design of image processing systems	- Examples of basic image processing systems. - Analysis of hardware resources required. - Implementation and performance analysis.
Theory: Theme 7. Design of audio processing systems	- Examples of audio processing systems. - Analysis of required hardware resources. - Implementation and performance analysis.
Theory: Theme 8. Design of signal processing systems for communications	- Examples of signal processing systems for communication applications. - Implementation and performance analysis.
Labs: Design of basic signal processing systems.	- Design, implementation and verification of basic signal processing systems described using VHDL: digital filters, communication applications, image processing, audio processing. - Using the ISE design tool from Xilinx and MATLAB from MathWorks.

Planning			
	Class hours	Hours outside the classroom	Total hours
Introductory activities	1	0	1
Laboratory practises	14	14	28
Projects	9	54	63
Master Session	14	14	28
Short answer tests	2	6	8
Jobs and projects	2	6	8
Practical tests, real task execution and / or simulated.	0	14	14
*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.			

Methodologies	
	Description
Introductory activities	The theoretical ad practical key topics of the subject, as well as the projects to be developed along the course will be presented by the teacher. CG6, CE39 and CE45 competencies will be worked on.
Laboratory practises	Basic signal processing systems will be implemented using FPGAs. CG6, CG9, CE39, CE45 and CG13 competencies will be worked on.

Projects	Working groups of two or more students will be established. Each group will develop two projects along the course. These projects will address the design of signal processing systems of low and medium complexity, respectively. Additionally, small groups (Groups Type C) will be available allowing monitoring the projects to be developed in the course. Activities to be developed in groups C: Activity 1. Description, analysis and discussion of the systems designed in the first project of the course. Presentation of results. Duscussion of design alternatives. Activity 2. Analysis and monitoring of the proposed solution for the second project. Activity 3. Demonstration of the behavior of systems designed in the second project. Analysis and discussion of results. CG6, CG9, CE39, C345, CG13, CT2, CG4 and CT4 competencies will be worked on.
Master Session	The theoretical content of the course and the introductory activities of both the theoretical and practical contents will be presented. CG6, CE39 and CE45 competencies will be worked on.

Personalized attention

Methodologies	Description
Master Session	The teacher will personally attend student□s doubts and queries related to theoretical contents. Students will have the opportunity to attend to individual or group tutorials, which will be held at the teacher's office following the schedule to be established at the beginning of the course, and to be published at the School of Telecommunications Engineering website.
Laboratory practises	The teacher will personally attend student□s doubts and queries related to laboratory practices and projects. Students will have the opportunity to attend to individual or group tutorials, which will be held at the teacher's office following the schedule to be established at the beginning of the course, and to be published at the School of Telecommunications Engineering website.
Projects	The teacher will personally attend student□s doubts and queries related to laboratory practices and projects. Students will have the opportunity to attend to individual or group tutorials, which will be held at the teacher's office following the schedule to be established at the beginning of the course, and to be published at the School of Telecommunications Engineering website. In adition, the projects asigned will be monitoring during the small groups (Groups Type C) activities.

Assessment

	Description	Qualification	Training and Learning Results
Short answer tests	There will be a short-answer test on the theoretical issues of the course. More information is provided in the "Other Comments" section below. This test will assess competencies CE39 and CE45.	20	C39 C45
Jobs and projects	There will be two projects during the course. In the first project the student will design a basic signal processing system. The weight of this assessment is 35% of the total grade for the course. The second project will involve the design of a signal processing system of medium complexity and its evaluation will be a 35% of the final grade. More information is provided in the "Other Comments" section that follows. These projects will assess competencies CG4, CG6, CG9, CG13, CE39, CE45, CT2 and CT4.	70	B4 B6 B9 B13 C39 C45 D2 D4
Practical tests, real task execution and / or simulated.	The laboratory practices will be continuously evaluated during laboratory hours (Type B hours). The weight of this assessment is 10% of the total grade for the course. These practices will assess competencies CG4, CG6, CG13, CE39, CE45 y CT4.	10	B4 B6 B13 C39 C45 D4

Other comments on the Evaluation

According to the guidelines for the degree programme , two evaluation systems will be offered to students: continuous

assessment and a final exam.

1.- Continuous assessment

The evaluation of the course is done through continuous assessment, which consists of a theory test, a set of laboratory practices and the delivery of two theoretical-practical works (projects). However, the realization of a final test is also included as an alternative.

The theoretical examination will include the contents of the first three temes of the course and will take place during lecture hours (Type A hours). The weight of this examination will be 2 points out of 10.

The laboratory practices will be performed in groups of two or more students and will be continuously evaluated during laboratory hours (Type B hours). The weight of this assessment is 1 point out of 10. The score will be the same for all the members of a working group.

The first theoretical-practical work will include themes 1 to 5. It will consist of the design of a basic signal processing sysem. This work will be conducted in laboratory and small groups hours (Type B and C hours) in groups of two or more students. As a result of the work a descriptive report of the designed system must be delivered. The weight of this assessment is 3.5 points out of 10.

The second theoretical-practical work will include themes 6 to 8. This work will be conducted in laboratory and small groups hours (Type B and C hours) in groups of two or more students. As a result of the work a descriptive report of the designed system must be delivered and the results discussed later (Type C hours). The weight of this assessment is 3.5 points out of 10 (3 points correspond to the execution and documentation tasks and 0.5 points to de presentation and discussion ones).

To carry out the two theoretical-practical works individual and cooperative tasks will be assigned to the students. The weight of the individual work will be the 60% of the maximum score of the project and the weight of the cooperative work will be the 40%. The 40% of the score corresponding the cooperative work will be the same for all the members of a working group.

The final grade for the course will be the sum of the four assessments. To pass the course a student must meet the following conditions:

- Get at least 5 out of 10 in the overall evaluation.

- Get at least 40% of the maximum score for each of the evaluation activities.

Students who fail any of the assessments shall be submitted to the corresponding final exam. Similarly, students who want to improve the grade obtained in any of the assessments may be submitted to final exam.

In the case a student fails to obtain at least 40% of the maximum score in any of the assessment activities, but has above the minimum of 5 out of 10 in the overall assessment, the student will be considered suspended and the note 4.5 will appear in the minutes.

It is understood that the student chooses continuous assessment if he/she conducts the two first laboratory practises, and since then will be considered submitted to this evaluation alternative.

2.- Assessment by final exam.

The final exam will consist of the same evaluative activities covered by continuous assessment. This means that on the date scheduled for the final exam students who have not opted for the continuous assessment should make the theoretical examination of the themes 1 to 3 of the course and deliver the reports of the laboratory practices and of both theoretical-practical works equivalent to that performed by continuous assessment. The theoretical-practical works will be discussed in the week following delivery.

As noted above, those students who have opted for continuous assessment and not passed any assessment activities or want to improve their grade may also pass a final exam only with the theme (or themes) to be considered. In this case the grade will be the highest between the final examination and continuous assessment.

3.- Second call (July)

The second call assessment exam will have two parts, a theoretical examination of the whole themes of the course and a practical one.

The theoretical examination would include short answer questions, problems, and/or system design exercises.

The practical examination will consist in the final test of a system previously designed and simulated. The student will demonstrate the proper functioning of the system using a FPGA based development board. The teacher will assign the

design work to the students at the beginning of the second quadmester. One week before the second call assessment date the student must deliver a descriptive report of the designed system as well as the simulation results.

Both parts of the second call assessment (theoretical examination and practical examination) will represent the 50% of the final grade for the course.

The final grade for the course will be the sum of the two assessments. To pass the course a student must meet the following conditions:

- Get at least 5 out of 10 in the overall evaluation.

- Get at least 40% of the maximum score for each of the evaluation activities.

In the case a student fails to obtain at least 40% of the maximum score in any of the assessment activities, but has above the minimum of 5 out of 10 in the overall assessment, the student will be considered suspended and the note 4.5 will appear in the minutes.

4.- Other comments

- The exams will be written in Spanish. The student can use the Spanish, English or Galician to answer the exam and for the reports, works or presentations.

- The grades obtained from the continuous assessment and final exams are only valid for the current academic year.

- The use of books, notes or electronic devices such as phones or computers is not permitted in any test or exam. Mobile phones must be turned off and be out of reach of the student.

- In case of plagiarism is detected in any of the reports/tasks/exams done/taken, the final score for the subject will be 'fail' (0) and the teachers will inform the School authorities so that they take the actions that they consider appropiate.

- In case of plagiarism or abandonment of a member of a work group is detected, his/her score will be 'fail' (0) and will not compute for the score of the rest of the group.

Sources of information

Basic Bibliography

U. Meyer-Baese, **Digital signal processing with Field Programmable Gate Arrays**, 3th ed., Springer-Verlag, 2007

James H. McClellan, Ronald W. Schafer, Mark A. Yoder, **Signal processing first**, 1st ed., Pearson Education International, 2003

XUP, University of Strathclyde and Steepest Ascent, **DSP for FPGA Primer**, 2011

Complementary Bibliography

John G. Proakis, Dimitris G. Manolakis, **Digital signal processing**, 4th ed., Pearson Education International, 2007

John G. Proakis, **Tratamiento digital de señales : principios, algoritmos y aplicaciones**, 4ª ed., Prentice Hall, 2007

Recommendations

Subjects that are recommended to be taken simultaneously

Programmable Electronic Circuits/V05G300V01502

Subjects that it is recommended to have taken before

Digital Electronics/V05G300V01402
Digital Signal Processing/V05G300V01304