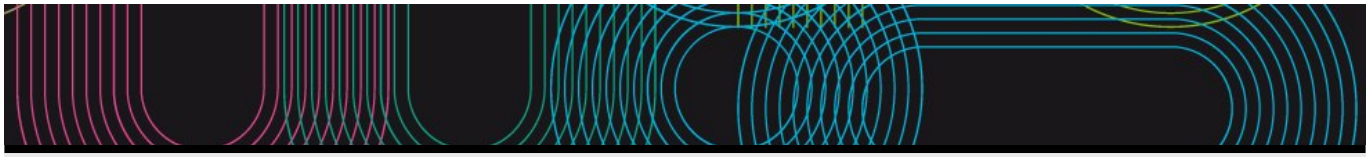

IDENTIFYING DATA				
Microelectronics Design				
Subject	Microelectronics Design			
Code	V05G300V01622			
Study programme	Degree in Telecommunications Technologies Engineering			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Optional	3rd	2nd
Teaching language	Spanish			
Department				
Coordinator	Cao Paz, Ana María			
Lecturers	Cao Paz, Ana María Rodríguez Pardo, María Loreto			
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General description	The main purposes of this course are for the students: 1) To get acquainted with integrated circuits (ICs) and micro-electro-mechanical systems (MEMs) fabrication technologies. 2) To get acquainted with CMOS fabrication processes for ICs and MEMs. 3) To analyze the physical structure of passive components and active devices in CMOS technology. 4) To get acquainted with the basic aspects of MEMs design. 5) To work with CAD tools for the design.of CMOS ICs			

Competencies	
Code	
B6	CG6: The aptitude to manage mandatory specifications, procedures and laws.
B9	CG9: The ability to work in multidisciplinary groups in a Multilanguage environment and to communicate, in writing and orally, knowledge, procedures, results and ideas related with Telecommunications and Electronics.
B13	CG13 The ability to use software tools that support problem solving in engineering.
C42	(CE42/SE4): The ability to apply electronics as support technology in other fields and activities and not only in information and communication technologies.
C43	(CE43/SE5): The ability to design analogical and digital electronics circuits of analogical to digital conversion and vice versa, of radiofrequency, of feeding and electrical energy conversion for computing and telecommunication engineering.
D4	CT4 Encourage cooperative work, and skills like communication, organization, planning and acceptance of responsibility in a multilingual and multidisciplinary work environment, which promotes education for equality, peace and respect for fundamental rights.

Learning outcomes			
Expected results from this subject	Training and Learning Results		
To know and understand integrated circuits (ICs) and micro-electro-mechanical systems (MEMs) fabrication processes.		C42	
To know and understand CMOS fabrication processes for ICs and MEMs, as well as the corresponding design methodologies and the steps in the development of an IC.	B6	C43	
To know and be capable of analizing the physical structure of resistors, capacitors, and transistors in CMOS technology.	B6 B9	C43	D4
To know and understand the basic aspects of MEMs design and their basic structures		C42	
To be capable of working with CAD tools for the design of CMOS ICs	B6 B9 B13		D4

Contents	
Topic	
Chapter 1: Introduction (1h)	Course introduction. Purposes and planning of the course. Basic concepts in the design of integrated circuits (ICs) and micro-electro-mechanical systems (MEMs).
Chapter 2: Fabrication steps for ICs and MEMs (2h)	Introduction to ICs and MEMs fabrication. Planar technology. Micromachining and micromolding technologies. CMOS IC fabrication steps. Structure of MOS transistors. Fabrication example: CMOS inverter. Layout. MEMs fabrication steps: bulk micromachining, surface micromachining, and LIGA.
Chapter 3. ICs and MEMs fabrication processes (3h)	Silicon wafers. Epitaxial layers. Dielectric layers. Oxidation. Deposition. Semiconductor layers. Dopant diffusion. Ion implantation. Photolithography. Etching. Metalization.
Chapter 4. Modeling of MOS transistors (3h).	MOS transistors: analytical model. Higher-order effects. Fundamentals of Spice modeling and simulatin. Spice models of MOS transistors.
Chapter 5. Physical structure of basic elements (2h)	Specification of the physical structure of a MOS transistor. Specification of the physical structure of a resistor. Specification of the physical structure of a capacitor. Types of physical specifications. Influence of physical design in the behavior of a device. Design rules. Design methodologies and tools.
Chapter 6. Resistor layout strategies (1h)	Lateral diffusion. Effective geometric dimensions. Influence of the terminals. Long resistors. Unit resistors. Stacked resistors. Neighborhood effects. Dummies. Interdigited and common centroid structures.
Chapter 7. Capacitor layout strategies (1h)	Oxide thickness gradient, lateral diffusion, and neighborhood effects. Area and perimeter unit capacitances.
Chapter 8. Transistor layout strategies (2h)	Transistor with high aspect ratio. Stacked transistors. Interdigited structures.
Chapter 9. Physical design case studies (3h)	Basic current mirror. Self-biased differential amplifier.
Lab assignment 1. Introduction to IC design tools (2h)	Introduction to physical design tools. Basic layout elements and individual nMOS and pMOS transistors. Design Rule Check (DRC). Predesigned elements and transistors.
Lab assignment 2. CMOS inverter (4h)	Schematic design of a CMOS inverter. Corrections for symmetrical response. Simulation with capacitive loads. Layout design and DRC. Layout Versus Schematic (LVS). Post-layout simulation (without and with capacitive load). Comparison with schematic simulation.
Lab assignment 3. MOS transsitor layout strategies (2h)	Layout of pMOS and nMOS transistors. Snake, stacked, and interdigited structures. Dummy structures.
Lab assignment 4. Physical design of analog functional blocks: current mirror and differential pair (3h)	Layouts of a basic curent mirror and a self-biased pMOS differential amplifier.
Lab assignment 5. Passive components layout strategies (2h)	Layouts of resistors and capacitors. Linear, snake, stacked and interdigited structures. Dummy structures.

Planning			
	Class hours	Hours outside the classroom	Total hours
Master Session	18	45	63
Practice in computer rooms	13	19.5	32.5
Projects	6	27	33
Presentations / exhibitions	1	2.5	3.5
Short answer tests	1	3.5	4.5
Troubleshooting and / or exercises	2	7	9
Practical tests, real task execution and / or simulated.	1	3.5	4.5
*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.			

Methodologies	
	Description
Master Session	The professor will present the relevant concepts of the course. Before each lecture, students must carry out a preparatory analysis of the topics to be addressed, aiming at their active participation. Practical examples and case studies will be developed and analyzed. Attendance will be recorded. Competencies CE42 and CE43 will be addressed in these sessions
Practice in computer rooms	Students will work in groups of two people, using IC CAD tools. All relevant steps in the physical design of an IC will be practically studied. Attendance will be recorded, and performance of each group in each lab assignment will be evaluated. Competencies CE43 and CG13 will be addressed in these sessions

Projects	Students will work in small teams (C-type groups) in the physical design and characterization of a circuit consisting of active devices and passive components, under the close guidance of professors. Attendance will be recorded. The activities to be developed by each team are: - Analysis of possible solutions and design alternatives. - Critical analysis of the design process developed. - Demonstration of the circuits designed in the project. - Preparation of a report where results are presented, analyzed, and discussed. Competencies CE43, CG6, CG9, CG13, and CT4 will be addressed in these sessions.
Presentations / exhibitions	Each group of students will publicly present their project to professors and the other students in the group. Anyone in the audience will be allowed to ask questions about the project. Competencies CE43, CG6, CG9, and CT4 will be addressed in these sessions.

Personalized attention

Methodologies	Description
Master Session	Professors will personally assist students with doubts and questions they may have about either theoretical contents. Office hours will be scheduled for both individual and group sessions.
Practice in computer rooms	Professors will personally assist students with doubts and questions they may have about lab assignments. Office hours will be scheduled for both individual and group sessions.
Projects	Professors will personally assist students with doubts and questions they may have about the development of the projects. Office hours will be scheduled for both individual and group sessions.
Presentations / exhibitions	Professors will personally assist students with doubts and questions they may have about the preparation of the public presentations. Office hours will be scheduled for both individual and group sessions.

Assessment

	Description	Qualification	Training and Learning Results
Projects	Each group of students will deliver the design carried out in the project in the format of the integrated circuit design tool. To pass the course, the design must meet technological standards and it shall comply the required specifications. In addition, each group must submit a detailed project report, with explicit information about the contribution of each of them to the whole, as well as the methodology followed for the distribution and coordination of tasks. Based on this division of tasks, it can be assigned an individual mark to each of the group members. The evaluation of the projects will be based on the following aspects: - Theoretical calculations carried out for design. - Analysis of design alternatives. - Successfully implementation and design verification for compliance with specifications. - Layout compaction. - Use of adequate layout strategies to minimize the effects of imperfections in the manufacturing process and to assure good matching of the electrical characteristics of the sets of components or devices that require it for functional reasons. - Formal issues: structure, clarity, conciseness, and completeness of the report. Use of suitable figures and discussion of significant data. Reports must be submitted on the date indicated in the planning of the course and it will be at least two days prior to the public presentation. To pass the course, students must achieve at least a mark of 5 or higher in a scale of 0-10 in the project (design and reporting). Competencies CE43, CG6, CG9, CG13, and CT4 will be assessed in these projects.	20	B6 C43 D4 B9 B13

Presentations / exhibitions	Each student must provide an individual 5-minute public presentation of the part of the project he/she carried out (including planning / coordination tasks, if applicable). Presentations will be scheduled in the last (1-hour) classroom session of the corresponding group. At the end of each presentation, the student must give suitable replies to questions from the audience, which will consist of professors and the other students in the group, who must attend the whole session. Evaluation will be based on the content, formal issues, and deliverance of the presentation, as well as on the way the student replies to que questions from the audience. Students asking relevant questions will get additional score for them. The mark obtained in the public presentation consists of two parts, a common part for tasks carried out jointly and an individual part of the exposition of each student of his or her work as well as the appropriate interventions at the end of the exposure of other groups. To pass the course, the student must achieve in his/her presentation (plus additional score if applicable) a mark of 5 or higher in a 0-10 scale. Competencies CE43, CG6, CG9, and CT4 will be assessed in these presentations.	10	B6 B9	C43 D4
Short answer tests	As part of the continuous assessment, two written individual tests are conducted. The first evaluation 1-hour written test will be held during one of the classroom sessions, covering course contents lectured so far. This test is the last chance for students to decide whether or not they opt for continuous evaluation. All students completing the test implicitly choose to follow continuous evaluation. The remaining students have to explicitly declare their choice. The lack of declaration from a student means he/she will not follow continuous evaluation. The test will consist of short answer questions, accounting for 20% of the global mark. The second written test will be held at the end of classroom sessions, covering the remaining classroom contents and accounting for 5% of the global mark. This test will be held in conjunction with the test of design problems or exercises more fully described below. The test will last for about an hour, including written test and design problems (or exercises) test. Both tests (covering the same course contents and with the same duration and evaluation criteria) will be held in the date of the final exam. They are compulsory for students not in continuous evaluation. Students in continuous evaluation can also voluntarily complete it. In that case, the score they will receive in this part of the course evaluation will be the one achieved in this second test. To pass the course, students must achieve in each of the tests a mark or 4 or higher in a 0-10 scale. Competencies CE42 and CE43 will be assessed in these tests	25		C42 C43
Troubleshooting and / or exercises	An exam of troubleshooting and / or exercises will be carried out as part of the continuous assessment, accounting for 15% of the global mark. This exam will be held in conjuction with the second written test described in the previous section and it will last for about an hour as a whole. Students in continuous evaluation can also voluntarily complete it again in the date of the final exam. In that case, the score they will receive in this part of the course evaluation will be the one achieved in this second test. For students not in continuous evaluation it is compulsory to carry out this exam (with the same structure, duration and evaluation criteria) on the date of the final exam. To pass the course, students must achieve in this exam a mark or 4 or higher in a 0-10 scale. Competencies CE42 and CE43 will be assessed in this test.	15		C42 C43
Practical tests, real task execution and / or simulated.	All students, in continuous evaluation or not, must complete Lab Assignment 2 and deliver a written report with the achieved results and conclusions. The report is due before the last scheduled lab session. Lab assignment 2 and the corresponding report account for 15% of the global mark. A continuous evaluation 1-hour lab test using an IC CAD tool will be held in the last scheduled lab session. Another similar test will be held in the date of the final exam. It is compulsory for students not in continuous evaluation. Students in continuous evaluation can also voluntarily complete it. In that case, the score they will receive in this part of the course evaluation will be the one achieved in this second test. Lab tests account for 15% of the global mark. To pass the course, students must achieve a mark or 4 or higher in a 0-10 scale in both Lab Assignment 2 and the lab test. Competencies CE43 and CG13 will be assessed in this part	30	B13	C43

Other comments on the Evaluation

In order to pass the course, students must achieve a global mark of 5 or higher in a 0-10 scale. The global mark will be obtained as the weighted summation of the scores obtained in the different parts of the course. A minimum score is required in each of these parts. For students not achieving the minimum score in any of the parts, the global mark will be the lower value between 4 and the weighted summation of scores.

Students not in continuous evaluation will be evaluated as follows:

- Final written and lab tests will account for the same percentage of the global mark as in the case of students in continuous evaluation.
- They must develop a project and deliver the corresponding report and public presentation (in the same sessions and with the same criteria as students in continuous evaluation). Reports are due two days before public presentation.
- They must complete Lab Assignment 2 and deliver a written report with the achieved results and conclusions.

Minimum scores in the different parts for students not in continuous evaluation are the same as for students in continuous evaluation.

Students not passing the course in the first call will have the opportunity to attend a second call. Requirements to pass the course will be the same as in the first call. In the second call, students must complete the two written tests and the lab test. No new projects and presentations will be allowed except for students not having achieved the minimum required scores on them. Project reports are due seven days before the date of the test.

Students who achieved the minimum scores in written and lab tests but not in project reports or presentations, will not need to complete the tests again, but only deliver project reports and presentations. However, they can voluntarily (in written) give up tests scores (at least seven days before the date of the second call) and complete all the tests again.

Sources of information

Basic Bibliography

José Antonio Rubio Solà, **Diseño de circuitos y sistemas integrados**,
Stephen A. Campbell, **Fabrication Engineering at the Micro-and Nanoscale**, 4ª,
J. Franca, Y. Tsividis (eds.), **Design of analog VLSI circuits for telecommunications and signal processing**,

Complementary Bibliography

Recommendations

Subjects that are recommended to be taken simultaneously

Analogue Electronics/V05G300V01624

Subjects that it is recommended to have taken before

Digital Electronics/V05G300V01402
Physics: Fundamentals of Electronics/V05G300V01305
Electronic Technology/V05G300V01401

Other comments

All conclusions achieved both in the written tests and in the projects must be adequately justified. Non-trivial concepts cannot be assumed but they have to be explained. The methodologies used by the student will be taken into account in the computation of his/her marks. No auxiliary resources, including but not limited to documentation, can be used in the written tests.