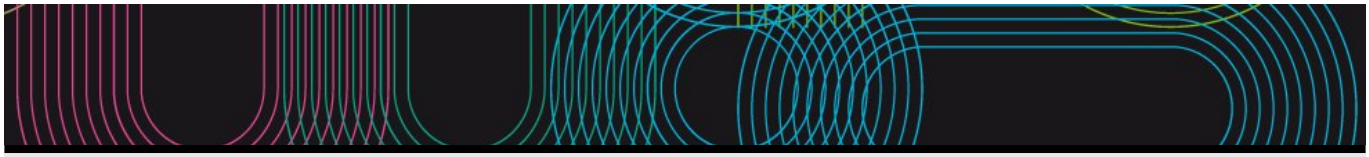

IDENTIFYING DATA				
Digital Electronics				
Subject	Digital Electronics			
Code	V05G300V01402			
Study programme	Degree in Telecommunications Technologies Engineering			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Mandatory	2nd	2nd
Teaching language	Spanish			
Department				
Coordinator	Machado Domínguez, Fernando			
Lecturers	Álvarez Ruiz de Ojeda, Luís Jacobo Machado Domínguez, Fernando Moure Rodríguez, María José Pérez López, Serafín Alfonso			
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General description	This course is an introduction to the basic principles of digital design and the analysis and design of digital circuits and systems. First, logic circuits, basic digital devices and logic gates representation will be introduced. Then, hardware description languages (HDL) based design, description and simulation methods will be described. Combinational and sequential logic design will be explained using the top-down design paradigm. Finally, the common combinational and sequential logic circuits will be described: operation, diagrams, symbols and VHDL description and simulation.			

Competencies	
Code	
B13	CG13 The ability to use software tools that support problem solving in engineering.
B14	CG14 The ability to use software tools to search for information or bibliographical resources.
C14	CE14/T9: The ability to analyze and design combinatory and sequential, synchronous and asynchronous circuits and the usage of integrated circuits and microprocessors.
C15	CE15/T10: The knowledge and application of the fundamentals of description languages for hardware devices.

Learning outcomes		
Expected results from this subject		Training and Learning Results
Knowledge of digital design principles, components and tools.		C14 C15
Ability to analyse and design combinational systems.	B13	C14 C15
Knowledge of the combinational functional blocks and their aplications.	B14	C14
Knowledge of the basic storage elements, the sequential blocks and their aplications.	B14	C14
Ability to analyse and design synchronous sequential systems.	B13	C14 C15
Knowledge of description and simulation methods based on hardware description languages (HDL).	B13	C14 C15

Contents	
Topic	
Unit 1: Introduction to digital electronics	Introduction to Digital Electronics. Number systems and digital codes. Boolean Algebra. Truth Tables. Logic Gates. Boolean Funtions Simplification.

Unit 2: Introduction to VHDL	Introduction to hardware description languages. Basic VHDL syntax. Data types and objects. Operators. Concurrent and sequential sentences. Component instantiation.
Unit 3: Basic combinational systems	Functional blocks. Technologies and output types of the digital circuits. Decoders. Encoders. Multiplexers. Demultiplexers. Application examples. VHDL description.
Unit 4: Programmable gate arrays	Introduction to the programmable circuits. PLA and PAL. Application examples.
Unit 5: Arithmetic combinational systems	Comparators. Parity detection and generation. Arithmetic circuits. Application examples. VHDL description.
Unit 6: Sequential logic systems principles	Definition and classification. Latches and flip-flops. Application examples. VHDL description.
Unit 7: Synchronous sequential systems	General theory. Counters. Multibit registers. Shift registers. Application examples. VHDL description.
Unit 8: Synchronous sequential logic design	Synchronous sequential systems design. Application examples. VHDL description.
Unit 10: Memory units	Classification. Active and pasive random access memories. Random access memories. Sequential acces memories. Associative memories.
Unit 9: Programmable logical devices	Introduction to the PLDs. Application examples.

PRACTICE 1. INTRODUCTION TO XILINX ISE	General ISE flow diagram. Schematic description. Practical examples.
PRACTICE 2. INTRODUCTION TO VHDL DESIGN	Description and synthesis of combinational systems using VHDL. Practical examples.
PRACTICE 3. DIGITAL SYSTEMS TEST: FUNCTIONAL SIMULATION	Obtaining symbols from schematic. Component instantiation. Stimulus definition. Test-bench Functional simulation. Practical examples.
PRACTICE 4. DIGITAL SYSTEMS COMPILATION AND IMPLEMENTATION. TEMPORAL SIMULATION	PLD architecture (Xilinx CoolRunner 2 family). Compilation and implementation. Temporal simulation. Practical examples.
PRACTICE 5. TESTING DIGITAL SYSTEMS TEST IN THE DEVELOPMENT BOARD	PLD development board CoolRunner 2 starter kit from Xilinx. Configuration file. PLD Technology and configuration methods. PLD programming. Digital systems test in the development board. Implementation examples.
PRACTICE 6. COMBINATIONAL CIRCUITS	Design and implementation of combinational circuits using VHDL: truth table, logic function and behavioural descriptions.
PRACTICE 7. ARITHMETIC CIRCUITS	Design and implementation of arithmetic circuits usign VHDL: truth table, logic function and behavioural descriptions.
PRACTICE 8. ARITHMETIC SYSTEMS	Design and implementation of arithmetic systems usign VHDL. Arithmetic and logic unit (ALU).
PRACTICE 9. SEQUENTIAL CIRCUITS I	Design and implementation of sequential circuits usign VHDL (flip-flops, registers and counters).
PRACTICE 10. SEQUENTIAL CIRCUITS II	Design and implementation of sequential circuits usign VHDL (counters, shift registers). Design and implementation of synchronous sequential logic systems usign VHDL (state machines).
PRACTICE 11. COMPONENT ASSEMBLY AND CONNECTION. DIGITAL INSTRUMENTATION.	Logic analyser. Connection of external push-buttons, switches, LEDs, 7-segments displays. Test of sequential circuits using the logic analyser.
PRACTICE 12. SEQUENTIAL SYSTEMS I	Design and implementation of a sequential system based on functional blocks usign VHDL. Dynamic controller of a 4-digit, 7-segment display.
PRACTICE 13. SEQUENTIAL SYSTEMS II	Design and implementation of a complex sequential system. Reading system of a row and column based button keypad .

Planning

	Class hours	Hours outside the classroom	Total hours
Introductory activities	1	1	2
Master Session	13	21	34
Laboratory practises	26	26	52
Troubleshooting and / or exercises	8	20	28
Practical tests, real task execution and / or simulated.	2	2	4
Troubleshooting and / or exercises	6	24	30

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies

	Description
Introductory activities	Subject presentation. Presentation of laboratory sessions, instrumentation and software resources to be used.

Master Session	The lecturer will explain in the classroom the main contents of the subject. The students have to manage the proposed bibliography to carry out a self-study process in a way that leads to acquire the knowledge and the skills related to the subject. The lecturer will answer the students questions in the classroom or in the office. In these sessions the students will develop the skils CE14 and CE15 ("know").
Laboratory practises	Activities designed to apply the main concepts and definitions of the subject. The students will be asked to acquire the basic skills to manage the laboratory instrumentation, software tools and components in order to construct and test electronic circuits. The students have to develop and demonstrate autonomous learning and collaborative skills. Possible questions can be answered in the laboratory sessions or in the lecturer s office. In these sessions the students will develop the skils CE15, CG13 and CG14 ("know how").
Troubleshooting and / or exercises	Activities designed to apply the main concepts of the subject to solve problems and exercices. The lecturer will explain a set of problems and the students have to solve diferent take-home sets of problems. The answers to selected problems will be provided later on. The lecturer will answer the students questions in the classroom or at the office. In these sessions the students will develop the skils CE14 and CG15 ("know how").

Personalized attention

Methodologies	Description
Master Session	The lecturer will answer the students questions and also give instructions to guide the studying and learning process. The students can go to the lecturer s office. The timetable will be available on the subject website at the beginning of the term.
Troubleshooting and / or exercises	The lecturer will answer the students questions and also give instructions to guide the studying and learning process. The students can go to the lecturer s office. The timetable will be available on the subject website at the beginning of the term.
Laboratory practises	The lecturer will answer the students questions and also give instructions to guide the studying and learning process. The students can go to the lecturer s office. The timetable will be available on the subject website at the beginning of the term.

Assessment

	Description	Qualification	Training and Learning Results	
Laboratory practises	The lecturer will check the level of compliance of the students with the goals related to the laboratory skills. Final mark of laboratory, FML, will be assessed in a 10 points scale. For the evaluation of the laboratory sessions, the lecturer will assess the group work (the same mark for each member) and the individual answers to personalized questions for each session (individual mark).	20	B13 B14	C15
Troubleshooting and / or exercises	The lecturer will check the students' skills to solve exercices and troubleshooting. Marks for each test will be assessed in a 10 points scale. Final mark of theory, FMT, will be assessed in a 10 points scale.	80		C14 C15

Other comments on the Evaluation

1. Continuous assessment

According to the guidelines of the degree and the agreements of the academic commission, a continuous assessment learning scheme will be offered to the students.

When the students perform a troubleshooting test or attend at least two laboratory sessions, ***they will be assessed by continuous assessment***.

The subject comprises two different parts: theory and laboratory. Once a task has been assessed, the students can not do/repeat the task at a later date. The marks are valid only for the current academic course.

1.a Theory

Three exercises and troubleshooting tests (ETT) are scheduled. The first and second test (ETT1 and ETT2) will be respectively performed after unit 4 and 7 (~ in weeks 6 and 12), in the usual weekly scheduling of the theoretical classes. The final test (FETT) will be performed during the examination period in the date specified in the academic calendar. Marks for each test will be assessed in a 10 points scale. In order to pass this part, students will be require to obtain at least a mark of 4 in the final test (FETT>=4). In this case the final mark of theory (FMT) will be:

FMT = max{FETT ; (0.2·ETT1 + 0.2·ETT2 + 0.6·FETT)}.

However, when the students do not pass the final test (FETT less than 4), the final mark of theory will be:

FMT = min{4 ; max{FETT ; (0.2·ETT1 + 0.2·ETT2 + 0.6·FETT)}}.

The students cannot do the tests at a later date. The student who miss a test will be assessed with a mark of 0 for that test.

1.b Laboratory

Thirteen laboratory sessions are scheduled. Each session lasts approximately 120 minutes and the students will work in pairs whenever possible. The first five sessions are guided practices. In these sessions, the instrumentation and software resources will be presented and the students will configure a programmable logic device following the design flow. These five sessions are mandatory but will not be assessed. The following seasons will be assessed by continuous assessment. Each session will be only evaluated according to the developed work at the schedule date. The marks for these laboratory sessions (LSM) will be assessed in a 10 points scale. The lecturer will consider the work of the students carried out before the laboratory session to prepare the proposed tasks, the work in the laboratory to deal with them as well as the student□s behavior. Only sessions 6 to 13 will be assessed. A mark of 0 will be obtained for missing sessions. In order to pass the laboratory part, the students can not miss more than two laboratory sessions. In this case, the weighted points from all assessed sessions are added together to calculate the final mark of laboratory (FML):

FML = (LSM6 + LSM7 + LSM8 + LSM9 + LSM10 + LSM11 + LSM12 + LSM13) / 8.

For the students who miss more than two laboratory sessions, the with a final mark of laboratory will be:

FML = min{4 ; (LSM6 + LSM7 + LSM8 + LSM9 + LSM10 + LSM11 + LSM12 + LSM13) / 8}.

1.c Final mark of the subject

The weighted points from all assessed parts are added together to calculate the final mark (FM). The following weightings will be applied: 80% theory (FMT) and 20% laboratory (FML). In order to pass the subject, students will be require to obtain at least a mark of 5 in each part (FMT>=5 and FML>=5). In this case the final mark (FM) will be:

FM = (0.8·FMT + 0.2·FML).

However, when the students do not pass both parts (FMT or FML less than 5), the final mark will be:

FM = min{4, (0.8·FMT + 0.2·FML)}.

A final mark higher than five points (FM >= 5) should be achieved in order to pass the subject.

2. Final exam

The students who prefer a different educational policy can attend an exam on a scheduled date. This exam consist on a theory part and laboratory part. In order to attend the laboratory exam, the students have to contact to the lecturer at least two weeks before the exam. This way, the organization of the laboratory exam will be simpler.

The theory exam will consist on an exercises and troubleshooting test (FETT). Mark for this test will be assessed in a 10 points scale. The final mark of theory (FMT) will be:

FMT = FETT.

The laboratory exam will consist on the resolution of a practical exercise in the laboratory. This practical exercise will be similar to those made in the laboratory sessions. The final mark of laboratory (FML) will be assessed in a 10 points scale.

In order to pass the subject, students will be required to pass the laboratory and theory exams. The minimum mark required

to pass each part is of 5 (FMT>=5 and FML>=5). In this case the final mark (FM) will be:

FM = (0.8·FMT + 0.2·FML).

However, when the students do not pass both parts (FMT or FML less than 5), the final mark will be:

FM = min{4 ; (0.8·FMT + 0.2·FML)}.

A final mark higher than five points (FM >= 5) should be achieved in order to pass the subject.

3. Second opportunity to pass the subject

This exam consist on a theory exam and a laboratory exam. Dates will be specified in the academic calendar. In order to attend the laboratory exam, the students have to contact to the lecturer at least two weeks before the final exam.

The marks obtained in the previous continuous assessment or final exam (FMT or FML) are kept for those parts in which the student has not attended. The final mark will be calculated as it has described in section 2 (final exam).

Sources of information

Basic Bibliography

L. J. Álvarez, F. Machado, M.J. Moure, S. Pérez, **Electrónica Digital**, Curso 2017-2018,

Wakerly J. F., **Digital Design. Principles and Practices**, 4ª,

E. Mandado, **Sistemas Electrónicos Digitales**, 10ª,

Complementary Bibliography

Thomas L. Floyd, **Fundamentos de Sistemas Digitales**, 11ª,

Wakerly J. F., **Diseño Digital. Principios y prácticas**, 3ª,

L.J. Álvarez, E. Mandado, M.D. Valdés, **Dispositivos Lógicos Programables y sus aplicaciones**, 1ª,

S. Pérez, E, Soto, S. Fernández, **Diseño de sistemas digitales con VHDL**,

L.J. Álvarez, **Diseño Digital con Lógica Programable**, 1ª,

Recommendations

Subjects that it is recommended to have taken before

Informatics: Computer Architecture/V05G300V01103
Physics: Fundamentals of Electronics/V05G300V01305