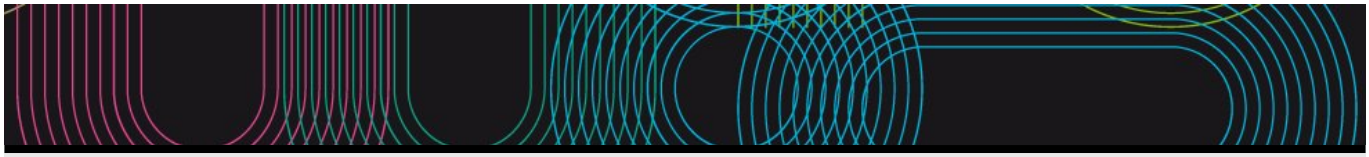

IDENTIFYING DATA				
Programmable Electronic Circuits				
Subject	Programmable Electronic Circuits			
Code	V05G300V01502			
Study programme	(*)Grao en Enxeñaría de Tecnoloxías de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Mandatory	3rd	1st
Teaching language	Spanish Galician			
Department				
Coordinator	Álvarez Ruíz de Ojeda, Luís Jacobo			
Lecturers	Álvarez Ruíz de Ojeda, Luís Jacobo Machado Domínguez, Fernando Moure Rodríguez, María José Poza González, Francisco Verdugo Mates, Rafael			
E-mail	jalvarez@uvigo.es			
Web	http://www.faitic.uvigo.es/			
General description	The main learning goals of this course are: Architecture of microprocessors, microcontrollers and configurable devices. Design methods and tools to acquire the necessary skills to design systems based on these devices.			

Competencies	
Code	
A3	CG3: The knowledge of basic subjects and technologies that capacitates the student to learn new methods and technologies, as well as to give him great versatility to confront and update to new situations
A4	CG4: The ability to solve problems with initiative, to make creative decisions and to communicate and transmit knowledge and skills, understanding the ethical and professional responsibility of the Technical Telecommunication Engineer activity.
A16	CE7/T2: The ability to use communication and software applications (ofimatics, databases, advanced calculus, project management, visualization, etc.) to support the development and operation of Electronics and Telecommunication networks, services and applications.
A17	CE8/T3: The ability to use software tools for bibliographical resources search or information related with electronics and telecommunications.
A23	CE14/T9: The ability to analyze and design combinatory and sequential, synchronous and asynchronous circuits and the usage of integrated circuits and microprocessors.
A24	CE15/T10: The knowledge and application of the fundamentals of description languages for hardware devices.
B4	The ability to use software tools that support problem solving in engineering

Learning aims		
Expected results from this subject	Training and Learning Results	
To understand the basic architecture of microprocessors, microcontrollers and configurable devices (FPGAs).	A3 A23 A24	
To study the methods and techniques of design of integrated hardware/software systems (System on Chip □ SoC).	A3 A23 A24	
To know the hardware and software tools for the design of systems based in programmable devices.	A3 A23 A24	B4

To handle the design tools for the design of systems based on programmable devices.	A23 A24	B4
To design simple integrated systems (System on Chip SoC) applied to the telecommunications fields.	A4 A16 A17 A23 A24	

Contents	
Topic	
LESSON 1 THEORY (1 h.). INTRODUCTION TO FPGAs.	1.1.- Introduction. 1.2.- Definition of FPGA. FPGA classification. 1.3.- FPGA architectures. 1.3.1.- Logical resources. 1.3.1.1.- Configurable Logic Blocks. 1.3.1.2.- Internal Logic Blocks. 1.3.1.3.- Input/Output Blocks. 1.3.1.4.- Embedded circuits. Memories. PLL digital circuits. Arithmetical circuits. Multipliers. DSP blocks. Serial transceivers. 1.3.2.- Interconnection resources. 1.3.2.1.- Interconnection lines. 1.3.2.2.- Configurable connection points. 1.3.3.- Examples of commercial FPGAs. 1.4.- FPGA technologies. 1.4.1.- FPGA manufacturing technologies (LVTTL, LVCMOS, etc.). 1.4.2.- FPGA configuration technologies. 1.4.2.1.- Static RAM technology (SRAM). 1.4.2.2.- Antifuse technology. 1.4.2.3.- Non-volatile memory technology (EEPROM). 1.4.3.- FPGA configuration. Methods. External programmer. In System Programmable (ISP). 1.5.- General characteristic of the FPGAs. 1.6.- Advantages of the FPGAs. 1.7.- Stages of the design of digital systems with FPGAs. 1.7.1.- Design implementation with FPGAs. 1.8.- FPGA CAD tools. 1.9.- FPGA applications. 1.10.- FPGAs versus other circuits. Comparative analysis.
LESSON 2 THEORY (1 h.). XILINX SPARTAN 3 FPGA FAMILY. ARCHITECTURE.	2.1.- Introduction. 2.2.- Xilinx Virtex 2 family architecture. 2.2.1.- Logical resources. CLBs. Slices. RAM-based shift registers. 2.2.2.- Internal memories. Distributed memory. Embedded memory. 2.2.3.- Clock circuits. 2.2.4.- Hardware multipliers. 2.2.5.- Input / Output technologies. 2.3.- Spartan 3 vs. Virtex 2. 2.4.- Spartan 3E vs. Spartan 3. 2.5.- Synthesis guidelines.
LESSON 3 THEORY (2 h.). INTRODUCTION TO MICROCONTROLLERS.	3.1.- Introduction. Definition of microcontroller. 3.2.- Internal architecture. Harvard. Von Neumann. 3.2.1.- Control Unit. 3.2.2.- ALU. 3.2.3.- Instruction set. RISC. CISC. 3.3.- External architecture. 3.3.1.- Access to memory. Program memory. Data memory. 3.3.2.- Access to peripherals. Input / Output ports. 3.3.3.- Interrupt control. 3.4.- Integrated peripherals. 3.4.1.- Timers. 3.4.2.- Serial communication. UART RS232. SPI. I2C. 3.4.3.- A/D and D/A converters. 3.5.- Examples of commercial microcontrollers. 3.6.- Microcontroller applications. 3.7.- Tools for programming and verification.
LESSON 4 THEORY (2 h.). XILINX PICOBLAZE MICROPROCESSOR (I).	4.1.- Introduction. 4.2.- Versions of the Xilinx Picoblaze microprocessor. 4.3.- Internal architecture of the Picoblaze microprocessor. 4.4.- Instruction set of the Picoblaze microprocessor.

LESSON 5 THEORY (1 h.). SOFTWARE DEVELOPMENT FOR XILINX PICOBLAZE MICROPROCESSOR.	5.1.- Introduction. 5.2.- Syntax of an assembler program for the Picoblaze microprocessor. 5.3.- Program development with pBlazeIDE environment for Picoblaze .
LESSON 6 THEORY (3 h.). XILINX PICOBLAZE MICROPROCESSOR (II).	6.1.- Introduction. 6.2.- External architecture. 6.2.1.- Input / Output instructions. 6.2.2.- Connection of input peripherals. 6.2.3.- Connection of output peripherals. 6.2.4.- Initial state. 6.2.5.- External interrupts. 6.3.- Design of peripherals for the Picoblaze microprocessor.
LESSON 7 THEORY (1 h.). INTRODUCTION TO SYSTEMS ON CHIP (SOC).	7.1.- Introduction to digital design methods. 7.1.1.- Software method. 7.1.2.- Hardware method. 7.2.- Systems On Chip (SOC). 7.3.- Systems On a Programmable Chip (PSOC). Microprocessors embedded in FPGAs. 7.3.1.- Hardware Microprocessors. 7.3.2.- Software Microprocessors. 7.4.- Embedded microprocessor applications.
LESSON 8 THEORY (3 h.). HARDWARE / SOFTWARE CODESIGN.	8.1.- Introduction. 8.2.- Software design. 8.3.- Hardware design. 8.4.- Stages of hardware / software codesign. 8.5.- Hardware / software partition. 8.6.- Examples hardware / software codesign. 8.7.- Peripheral design. How to split functions between □hardware□ and □software□.
LESSON 9 THEORY (4 h.). DESIGN OF COMPLEX SYSTEMS.	9.1.- Introduction. 9.2.- Previous analysis of the most suitable solution. 9.3.- Application specific peripherals. Design methods. 9.3.1.- Practical examples.
LESSON 10 THEORY (2 h.). INTRODUCTION TO CORRECT DESIGN METHODS.	10.1.- Introduction. 10.2.- Design of digital systems with FPGAs. 10.2.1.- Hierarchical design. 10.2.2.- Independent technology design. 10.2.3.- Timing design.
LESSON 11 THEORY (4 h.). SYNCHRONOUS DIGITAL SYSTEM DESIGN.	11.1.- Introduction. 11.2.- Synchronous design. 11.3.- Synchronous sequential systems. FPGA design tips. 11.4.- Synchronisation of input variables.
LESSON 1 LABORATORY (2 h.). STAGES OF DIGITAL SYSTEM DESIGN WITH FPGAs.	1.1.- Introduction. Xilinx ISE tool flow diagram. 1.2.- VHDL description. 1.3.- Behavioural simulation. 1.4.- Synthesis. 1.5.- Implementation. 1.6.- Implementation options for the Xilinx Spartan 3E FPGA family. 1.7.- FPGA Editor. 1.8.- Timing simulation. 1.9.- Timing analysis report. 1.10.- Technology and configuration methods for Xilinx FPGAs. 1.11.- Development boards based on FPGAs of Xilinx. 1.12.- Configuration file (.BIT). 1.13.- FPGA programming. □iMPACT□. 1.14.- Digital system testing. Frequent problems. 1.15.- Examples.
LESSON 2 LABORATORY (2 h.). PERIPHERAL CIRCUIT DESIGN FOR THE PICOBLAZE MICROPROCESSOR.	2.1.- Introduction. 2.2.- Guidelines on synchronous design with VHDL. 2.3.- Basic register in VHDL. 2.4.- Data memory in VHDL. 2.5.- Timer in VHDL.
LESSON 3 LABORATORY (2 h.). PERIPHERALS INTERFACE CIRCUIT DESIGN FOR THE PICOBLAZE MICROPROCESSOR.	3.1.- Introduction. 3.2.- Input peripheral interface circuit in VHDL. 3.3.- Output peripheral interface circuit in VHDL. 3.4.- Interrupt storing circuit in VHDL.
LESSON 4 LABORATORY (2 h.). XILINX PICOBLAZE MICROPROCESSOR SOFTWARE TOOLS.	4.1.- Introduction. 4.2.- Program assembler and simulator in Mediatronix. Picoblaze IDE. 4.3.- Basic examples.

LESSON 5 LABORATORY (6 h.). DESIGN OF DIGITAL SYSTEMS BASED ON THE PICOBLAZE MICROPROCESSOR.	5.1.- Introduction. 5.2.- Picoblaze microprocessor source files. 5.3.- Design stages for digital systems based on the Picoblaze microprocessor. 5.3.1.- Choosing the right Picoblaze microcontroller. 5.3.2.- Picoblaze program design. 5.3.3.- Picoblaze program simulation. 5.3.4.- Generation of the necessary VHDL files for the implementation of the Picoblaze Microprocessor in Xilinx Spartan 3E FPGA family. 5.3.5.- Peripheral circuit design for the Picoblaze microcontroller. Additional circuits needed. 5.3.6.- Simulation of the peripheral and additional circuits. 5.3.7.- Implementation of the complete digital system. 5.3.8.- Test of the complete digital system. 5.4.- Design of a basic example with use of interrupts, based on the Picoblaze microprocessor.
LESSON 6 LABORATORY (12 h.). PROJECTS. DESIGN OF DIGITAL SYSTEMS BASED ON THE PICOBLAZE MICROPROCESSOR.	6.1.- Design and implementation of a medium-complexity digital system based on the Picoblaze 3 microprocessor, according to the instructions supplied by the teacher through FaiTIC website.

Planning

	Class hours	Hours outside the classroom	Total hours
Master Session	12	16	28
Troubleshooting and / or exercises	12	19	31
Laboratory practises	14	20	34
Tutored works	12	24	36
Introductory activities	2	2	4
Short answer tests	4	13	17
*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.			

Methodologies

	Description
Master Session	Conventional lectures. Through this methodology the outcome CG3 is developed.
Troubleshooting and / or exercises	These sessions will include the realisation of exercises and works by part of the professor and of the students. Through this methodology the outcomes CG3, CG4, CE8/T3, CE14/T9 and CE15/T10 are developed.
Laboratory practises	VHDL design of digital circuits and development of assembler programs. Implementation in FPGAs. Through this methodology the outcomes CG3, CG4, CG13, CE7/TE2, CE8/T3, CE14/T9 and CE15/T10 are developed.
Tutored works	The students must design the circuits and programs needed to build a complete embedded system based on a FPGA. Through this methodology the outcomes CG3, CG4, CG13, CE7/TE2, CE8/T3, CE14/T9 and CE15/T10 are developed.
Introductory activities	Introduction to the subject key topics both theoretical and practical. Through this methodology the outcome CG3 is developed.

Personalized attention

Methodologies	Description
Laboratory practises	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.
Tutored works	In class the teacher will assist the students. Besides, the students will have the opportunity to consult with the teacher in office hours which will be published in the faculty website.

Assessment

Description	Qualification

Laboratory practises	Design of digital circuits in VHDL and assembler programs. It will be necessary to deliver the design source files and to show the teacher the correct operation of each one of the circuits and programs.. The assessment will be based on the operation of the circuits and programs developed in the practical sessions corresponding to the laboratory lessons 1 to 5, according to the published criteria. Through this methodology the outcomes CG3, CG4, CG13, CE7/TE2, CE8/T3, CE14/T9 and CE15/T10 are assessed.	25
Tutored works	Autonomous Project. Design of a medium-complexity embedded digital system with at least a complex peripheral designed by the students. It will be necessary to deliver the design source files and a report of maximum 10 pages, describing the work done, according to the index supplied by the professor. The content corresponds with laboratory lesson 6. The assessment will be based on the operation of the digital system and the correct application of the theoretical concepts, according to the published criteria. Through this methodology the outcomes CG3, CG4, CG13, CE7/TE2, CE8/T3, CE14/T9 and CE15/T10 are assessed.	25
Short answer tests	Two exams based on multiple choice questions or short questions about the theoretical topics of the subjects. Through this methodology the outcomes CG3, CG4, CE14/T9 and CE15/T10 are assessed.	50

Other comments on the Evaluation

The total mark will be the sum of the marks obtained in the different tasks of the subject.

The mark of each one of the theoretical exams has to be equal or greater than 5 over 10 in order to pass the subject.

The global mark of the laboratory guided practices has to be equal or greater than 5 over 10 in order to pass the subject.

The mark of the practical work has to be equal or greater than 5 over 10 in order to pass the subject.

All the students, both those who follow the subject continuously and those who want to be assessed in the final exam at the end of the term or at the end of the year (second opportunity), will have to do the tasks described in the previous section.

The students that do not attend classes regularly will also have to do the same tasks as the students who attend classes.

The final mark will be expressed in numerical form ranging from 0 to 10, according to the valid regulation (Royal decree 1125/2003 of 5 September; BOE 18 September).

Following the guidelines of the degree the students will be offered two assessment systems: continuous assessment and final assessment at the end of the term.

CONTINUOUS ASSESMENT:

The students are considered to have chosen the continuous assessment when they have done 2 laboratory practices and/or have sat the first theoretical examination.

The students who want to be assessed in the continuous assessment can only miss two sessions as a maximum. If they miss more than 2 sessions, it will be compulsory to do an additional individual task or an examination.

The students that have chosen continuous assessment, but do not pass the course, will have to do the final assessment at the end of the year (second opportunity), that is, will have to repeat all the tasks, included those that had passed.

The students that pass the course by means of continuous assessment will not be allowed to repeat any task in the final assessment in order to improve the mark.

The different tasks should be delivered in the date specified by the teacher, otherwise they will not be assessed for the continuous assessment.

The students will develop the theoretical exercises, the laboratory practices and the laboratory projects in groups of two students during the continuous assessment.

FINAL ASSESMENT:

The students that opt for the final assessment will have to do all the theoretical and practical tasks and the project individually.

The tasks for the final assessment have to be delivered before the official date of the examination set by the faculty.

In case the students pass the four tasks (mark of each task >= 5), the final mark (FM) will be the weighted sum of the marks of each part of the subject:

FM = 0'25 * TE1 + 0'25 * TE2 + 0'25 * LP + 0'25 * AP

In case the students do not pass any of the four tasks of the subject(mark of some task < 5), the final mark (FM) will be:

FM = Minimum [4'5; (0'25 * TE1 + 0'25 * TE2 + 0'25 * LP + 0'25 * AP)]

Being:

TE1 = First partial theoretical examination.

TE2 = Second partial theoretical examination.

LP = Global mark of the guided Laboratory Practices corresponding to the lessons 1 to 5.

AP = Laboratory Autonomous Project.

ASSESSMENT CRITERIA.

1) Theoretical examinations.

The first theoretical examination will be scheduled around the sixth week of classes in the place and date determined by the professors and the faculty. At least, it will be scheduled after having studied the theoretical lessons 1 to 8.

The second theoretical examination will be scheduled around the fourteenth week of classes in the place and date that determined by the professors and the faculty.

The students will have to properly answer the exam questions.

2) Laboratory guided practices.

The correct operation of the circuits and programs developed in the laboratory sessions will be evaluated, according to the marks stated in the practice bulletin. Each practical lesson will be marked over 10. Afterwards, its influence will be weighted in the total mark of the subject, according to the number of hours assigned to each lesson. As a consequence, the global mark of the practices corresponding to the lessons 1 to 5 of laboratory, is obtained through the following equation:

LP = (Practice 1L Mark + 2 * Practice 2L Mark + Practice 3L Mark + Practice 4L Mark + 2 * Practice 5L Mark) / 7

The total mark of the guided laboratory practices (LP) corresponds to 25% of the total mark of the subject.

It will be necessary to deliver the required source files.

The assessment criteria refer only to the functionality of the circuits and programs developed, that is, the circuits and programs have to work perfectly in all his aspects to obtain the maximum mark, whether it is the software simulation, the behavioural and timing simulation of the different hardware circuits and complete system, or the test in the development board.

3) Autonomous laboratory work.

Autonomous project. The students must design a medium-complexity embedded system with at least a complex peripheral designed by the students. It will be necessary to deliver a short report on the work done.

The assessment criteria of the autonomous work are the following:

1) Suitable hardware / software partitioning.

2) Suitable hardware organisation and suitable assembler program structure.

3) Design correctness.

Optimisation of the VHDL description and circuit use.

Application of synchronous design techniques.

4) Analysis of the FPGA implementation.

Analyse the FPGA logical resources used and their justification.

Analyse the internal system delays.

5) Functionality.

Software simulation.

Behavioural simulation of the different hardware circuits.

Simulation of the complete embedded system (hardware + software).

Board test of the complete embedded system (hardware + software).

All the sections have to work perfectly to obtain the maximum mark.

6) Documentation of the design and FPGA implementation.

a. Report.

i. Clear structure and order.

ii. Clear explanations.

iii. Enough explanations to understand the work done.

iv. Inclusion of suitable figures.

v. Inclusion of relevant data.

b. Source design files.

i. Enough comments in the VHDL files to explain the sentences used.

ii. Enough comments in the assembler files to be understood.

Sources of information

[POZA et AL 12] POZA GONZÁLEZ, F., ÁLVAREZ RUIZ DE OJEDA, L.J., *Diseño de sistemas*

COMPLEMENTARY BIBLIOGRAPHY OF THE SUBJECT:

DIGITAL SYSTEM DESIGN:

[ÁLVAREZ 02] ÁLVAREZ RUIZ DE OJEDA, L. Jacobo, MANDADO PÉREZ, E., VALDÉS PEÑA, M.D., *Dispositivos Lógicos Programables y sus aplicaciones*, Editorial Thomson-Paraninfo, 2002.

[BOLTON 90] BOLTON, M., "*Digital systems design with programmable logic*", Addison-Wesley, 1990.

[SCARPINO 98] SCARPINO, F., *VHDL and AHDL digital system implementation*, Prentice Hall, Londres, 1998.

[ALTERA] Dirección de Internet, *http://www.altera.com*, Altera.

[JENKINS 94] JENKINS, Jesse H., "*Designing with FPGAs and CPLDs*", Prentice Hall, New Jersey, 1994.

[QUICKLOGIC] Dirección de Internet, *http://www.quicklogic.com*, Quicklogic.

MICROPROCESSORS:

[CHU 08] CHU, PONG P., *FPGA prototyping by VHDL examples : Xilinx Spartan-3 version*, John Wiley & Sons, Hoboken (New Jersey), 2008.

VHDL:

Recommendations

Subjects that continue the syllabus

Design and Synthesis of Digital Systems/V05G300V01923

Subjects that it is recommended to have taken before

Programming I/V05G300V01205
Digital Electronics/V05G300V01402
Physics: Fundamentals of Electronics/V05G300V01305

Other comments

The students will have previously followed the subject Digital Electronics. It gives the necessary knowledge to understand the topics of this course. It is not necessary to have passed it.

Besides, it is recommended that the students have previously followed the subject Physical: Foundations of Electronics and Programming I. They give the necessary knowledge to understand some topics of this course.