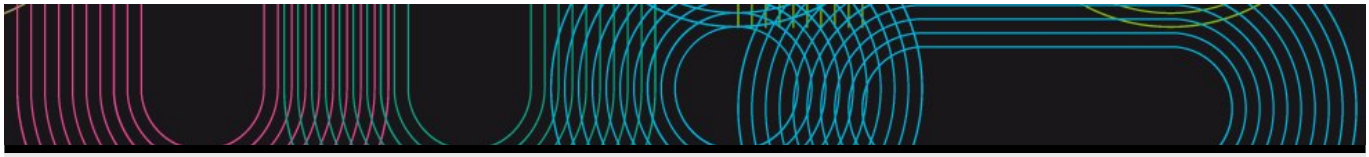

IDENTIFYING DATA				
(*)Deseño microelectrónico				
Subject	(*)Deseño microelectrónico			
Code	V05G300V01622			
Study programme	(*)Grao en Enxeñaría de Tecnoloxías de Telecomunicación			
Descriptors	ECTS Credits	Choose	Year	Quadmester
	6	Mandatory	3rd	2nd
Teaching language	Spanish			
Department				
Coordinator	Rodríguez Andina, Juan José			
Lecturers	Cao Paz, Ana María Fariña Rodríguez, Jose Rodríguez Andina, Juan José Rodríguez Pardo, María Loreto			
E-mail	jjrdguez@uvigo.es			
Web	http://faitic.uvigo.es			
General description	The main purposes of this course are for the students: 1) To get acquainted with integrated circuits (ICs) and micro-electro-mechanical systems (MEMs) fabrication technologies. 2) To get acquainted with CMOS fabrication processes for ICs and MEMs. 3) To analyze the physical structure of passive components and active devices in CMOS technology. 4) To get acquainted with the basic aspects of MEMs design. 5) To work with CAD tools for the design.of CMOS ICs			

Competencies

Code	
A9	CG9: The ability to work in multidisciplinary groups in a Multilanguage environment and to communicate, in writing and orally, knowledge, procedures, results and ideas related with Telecommunications and Electronics.
A51	(CE42/SE4): The ability to apply electronics as support technology in other fields and activities and not only in information and communication technologies.
A52	(CE43/SE5): The ability to design analogical and digital electronics circuits of analogical to digital conversion and vice versa, of radiofrequency, of feeding and electrical energy conversion for computing and telecommunication engineering.
B4	The ability to use software tools that support problem solving in engineering

Learning aims

Expected results from this subject	Training and Learning Results	
To know and understand integrated circuits (ICs) and micro-electro-mechanical systems (MEMs) fabrication technologies.	A51	
To know and understand CMOS fabrication processes for ICs and MEMs, as well as the corresponding design methodologies and the steps in the development of an IC.	A52	
To know and be capable of analizing the physical structure of resistors, capacitors, and transistors in CMOS technology.	A52	
To know and understand the basic aspects of MEMs design and their basic structures	A51	
To be capable of working with CAD tools for the design of CMOS ICs	A9	B4

Contents

Topic

Chapter 1: Introduction (1h)	Course introduction. Purposes and planning of the course. Basic concepts in the design of integrated circuits (ICs) and micro-electro-mechanical systems (MEMs).
Chapter 2: Fabrication steps for ICs and MEMs (2h)	Introduction to ICs and MEMs fabrication. Planar technology. Micromachining and micromolding technologies. CMOS IC fabrication steps. Structure of MOS transistors. Fabrication example: CMOS inverter. Layout. MEMs fabrication steps: bulk micromachining, surface micromachining, and LIGA.
Chapter 3. ICs and MEMs fabrication processes (3h)	Silicon wafers. Epitaxial layers. Dielectric layers. Oxidation. Deposition. Semiconductor layers. Dopant diffusion. Ion implantation. Photolithography. Etching. Metalization.
Chapter 4. CMOS process parameters (3h).	MOS transistors: analytical model. Higher-order effects. Spice model. Technology file. Parameters of a sample CMOS process.
Chapter 5. Physical structure of basic elements (2h)	Specification of the physical structure of a MOS transistor. Specification of the physical structure of a resistor. Specification of the physical structure of a capacitor. Types of physical specifications. Influence of physical design in the behavior of a device. Design rules. Design methodologies and tools.
Chapter 6. Resistor layout strategies (1h)	Lateral diffusion. Effective geometric dimensions. Influence of the terminals. Long resistors. Unit resistors. Stacked resistors. Neighborhood effects. Dummies. Interdigited and common centroid structures.
Chapter 7. Capacitor layout strategies (1h)	Oxide thickness gradient, lateral diffusion, and neighborhood effects. Area and perimeter unit capacitances.
Chapter 8. Transistor layout strategies (2h)	Transistor with high aspect ratio. Stacked transistors. Interdigited structures.
Chapter 9. Physical design case studies (3h)	Basic current mirror. Self-biased differential amplifier.
Lab assignment 1. Introduction to IC design tools (3h)	Basic layout elements. Design Rule Check (DRC). Extraction. Basic layout elements from libraries.
Lab assignment 2. MOS transistors (3h)	Layout of pMOS and nMOS transistors. Transistors from libraries. Snake, stacked, and interdigited structures. Dummy definition layers.
Lab assignment 3. Passive components (2h)	Layouts of resistors and capacitors. Resistors and capacitors from libraries. Linear, snake, stacked and interdigited structures.
Lab assignment 4. CMOS inverter (1h)	Schematic and layout of a CMOS inverter. Layout Versus Schematic (LVS). Layout extraction. Post-layout simulation.
Lab assignment 5. Current mirror (2h)	Schematic and layout of a basic curent mirror with resistive load and ideal input current source. LVS. Layout extraction.
Lab assignment 6. Differential amplifier (2h)	Schematic and layout of a self-biased pMOS differential amplifier. LVS. Layout extraction.

Planning

	Class hours	Hours outside the classroom	Total hours
Master Session	18	45	63
Practice in computer rooms	13	19.5	32.5
Projects	6	27	33
Presentations / exhibitions	1	2.5	3.5
Short answer tests	1	3.5	4.5
Troubleshooting and / or exercises	2	7	9
Practical tests, real task execution and / or simulated.	1	3.5	4.5

*The information in the planning table is for guidance only and does not take into account the heterogeneity of the students.

Methodologies

	Description
Master Session	The professor will present the relevant concepts of the course. Before each lecture, students must carry out a preparatory analysis of the topics to be addressed, aiming at their active participation. Practical examples and case studies will be developed and analyzed. Attendance will be recorded.
Practice in computer rooms	Students will work in groups of two people, using IC CAD tools. All relevant steps in the physical design of an IC will be practically studied. Attendance will be recorded, and performance of each group in each lab assignment will be evaluated.

Projects	Students will work in small teams (C-type groups) in the physical design and characterization of a circuit consisting of active devices and passive components, under the close guidance of professors. Attendance will be recorded. The activities to be developed by each team are: - Analysis of possible solutions and design alternatives. - Critical analysis of the design process developed. - Demonstration of the circuits designed in the project. - Preparation of a report where results are presented, analyzed, and discussed.
Presentations / exhibitions	Each group of students will publicly present their project to professors and the other students in the group. Anyone in the audience will be allowed to ask questions about the project.

Personalized attention

Methodologies	Description
Master Session	Professors will personally assist students with doubts and questions they may have about either theoretical contents or lab assignments, as well as in the development of the projects and the preparation of the public presentations. Office hours will be scheduled for both individual and group sessions.
Practice in computer rooms	Professors will personally assist students with doubts and questions they may have about either theoretical contents or lab assignments, as well as in the development of the projects and the preparation of the public presentations. Office hours will be scheduled for both individual and group sessions.
Projects	Professors will personally assist students with doubts and questions they may have about either theoretical contents or lab assignments, as well as in the development of the projects and the preparation of the public presentations. Office hours will be scheduled for both individual and group sessions.
Presentations / exhibitions	Professors will personally assist students with doubts and questions they may have about either theoretical contents or lab assignments, as well as in the development of the projects and the preparation of the public presentations. Office hours will be scheduled for both individual and group sessions.

Assessment

	Description	Qualification
Projects	Each group of students must deliver a detailed written report about the project they developed. Contributions from each team member must be clearly stated and identified. The methodology used for task distribution and coordination within the group must also be clearly explained. Evaluation will be based on: - Analysis of design alternatives - Design correctness - Layout compaction - Use of adequate layout strategies to minimize the effect of process variations and to assure good matching wherever required. - Formal issues: structure, clarity, conciseness, and completeness of the report. Use of suitable figures and discussion of significant data. Reports are due two days before the public presentation of the work. To pass the course, the group the student belongs to must achieve in the report a mark of 5 or higher in a 0-10 scale. Competencies A9, A52, and B4 will be assessed in these projects	15
Presentations / exhibitions	Each student must provide an individual 5-minute public presentation of the part of the project he/she carried out (including planning / coordination tasks, if applicable). Presentations will be scheduled in the last (1-hour) classroom session of the corresponding group. At the end of each presentation, the student must give suitable replies to questions from the audience, which will consist of professors and the other students in the group, who must attend the whole session. Evaluation will be based on the content, formal issues, and deliverance of the presentation, as well as on the way the student replies to que questions from the audience. Students asking relevant questions will get additional score for them. To pass the course, the student must achieve in his/her presentation (plus additional score if applicable) a mark of 5 or higher in a 0-10 scale. Competencies A9 and A52 will be assessed in these presentations	15

Short answer tests	An intermediate continuous evaluation written short answer 1-hour test will be held during one of the classroom sessions. This test is the last chance for students to decide whether or not they opt for continuous evaluation. All students completing the test implicitly choose to follow continuous evaluation. The remaining students have to explicitly declare their choice. The lack of declaration from a student means he/she will not follow continuous evaluation. Another test (covering the same course contents, and with the same duration and evaluation criteria) will be held in the date of the final exam. It is compulsory for students not in continuous evaluation. Students in continuous evaluation can also voluntarily complete it. In that case, the score they will receive in this part of the course evaluation will be the one achieved in this second test. To pass the course, students must achieve in this part a mark or 4 or higher in a 0-10 scale. Competencies A51 and A52 will be assessed in these tests	20
Troubleshooting and / or exercises	A 2-hour written test where students have to solve a design problem will be held in the date of the final exam. It is compulsory for all students, being or not in continuous evaluation. To pass the course, students must achieve in this part a mark or 4 or higher in a 0-10 scale. Competencies A51 and A52 will be assessed in this test	30
Practical tests, real task execution and / or simulated.	A continuous evaluation 1-hour lab test using an IC CAD tool will be held in the last scheduled lab session. Another similar test will be held in the date of the final exam. It is compulsory for students not in continuous evaluation. Students in continuous evaluation can also voluntarily complete it. In that case, the score they will receive in this part of the course evaluation will be the one achieved in this second test. To pass the course, students must achieve in this part a mark or 4 or higher in a 0-10 scale. Competencies A52 and B4 will be assessed in these tests	20

Other comments on the Evaluation

In order to pass the course, students must achieve a global mark of 5 or higher in a 0-10 scale. The global mark will be obtained as the weighted summation of the scores obtained in the different parts of the course. A minimum score is required in each of these parts. For students not achieving the minimum score in any of the parts, the global mark will be the lower value between 4 and the weighted summation of scores.

Students not in continuous evaluation will be evaluated as follows:
- The final written short answer test will account for 20% of the global mark.
- The final written design problem test will account for 30% of the global mark.
- The final lab test will account for 20% of the global mark.
- They must develop a project, and deliver the corresponding report and public presentation (in the same sessions and with the same criteria as students in continuous evaluation). Reports are due two days before the public presentation. The report and the public presentation will account for 15% of the global mark each.

Minimum scores in the different parts for students not in continuous evaluation are the same as for students in continuous evaluation.

Students not passing the course in the first call will have the opportunity to attend a second call. Requirements to pass the course will be the same as in the first call. In the second call, students must complete the two written tests and the lab test. No new projects and presentations will be allowed except for students not having achieved the minimum required scores on them. Project reports are due two days before the date of the test.

Sources of information

José Antonio Rubio Solà, **Diseño de circuitos y sistemas integrados**,
Stephen A. Campbell, **Fabrication Engineering at the Micro-and Nanoscale**, 3ª,
J. Franca, Y. Tsividis (eds.), **Design of analog VLSI circuits for telecommunications and signal processing**,

Recommendations

Subjects that are recommended to be taken simultaneously

(*)Electrónica analóxica/V05G300V01624

Subjects that it is recommended to have taken before

(*)Electrónica dixital/V05G300V01402

(*)Física: Fundamentos de electrónica/V05G300V01305
(*)Tecnoloxía electrónica/V05G300V01401

Other comments

All conclusions achieved both in the written tests and in the projects must be adequately justified. Non-trivial concepts cannot be assumed but they have to be explained. The methodologies used by the student will be taken into account in the computation of his/her marks. No auxiliary resources, including but not limited to documentation, can be used in the written tests.